GE SiC Devices and Modules for Aviation Applications

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Presented at CFES Conference, April 10, 2019, Troy, NY

SiC Driving the Next Power Revolution

Higher efficiency AND higher power density

Server PS: > 5% datacenter-level energy savings

UPS: >5%, datacenter-level energy savings footprint -25%

PV inverter: > 50% lower losses

Wind converter: > 50% lower losses

Aircraft electric power: 500kg lower weight

Electric locomotive: 5% lower weight

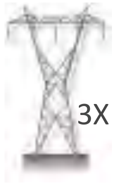
MV motor drive: >25% smaller footprint

Electric propulsion: ~ 10% less fuel consumed

New capabilities

Ship electric power distribution: 10x lower transformer weight

MRI, CT: better image quality, maller footprint



MV/HV grid applications: 3X fewer devices for SiC vs. Si

Oil and gas: New capability in hot & harsh conditions

Applications range from KW to MW

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GE SiC Advantage

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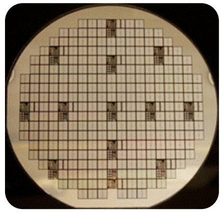
GE SiC Milestones

2011

Pilot 4” fab @ GE-GRC Demo’d MOSFETs with V_{TH} stable @200°C



2012

75kW, 20kHz Aviation inverter, **98.5% efficiency**

2013

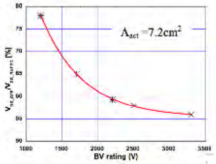
Industry-first 200°C **1.2kV, 115mΩ Gen1 qual. per AEC-Q101**

2014

Implemented QMS **ISO9001-2008** for GE 4” SiC pilot fab

2015

1[st] in SiC industry to quantify **TCR-related FIT vs. applied V_{DC}**



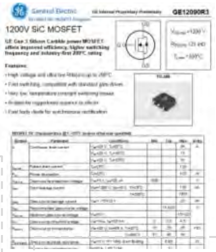
2016

200°C rated surface mount **1.2kV, 50mΩ Gen1 AEC-Q101 qual**

Fielded world’s first 1MW SiC converter: η_{pk} >99%, air-cooled

2017

200°C rated surface mount **1.2kV, 25mΩ Gen3 AEC-Q101 qual**



2018

Benchmark ultra-low inductance module for hi-perf. MW app’s

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Summary

SiC MOSFET Chip

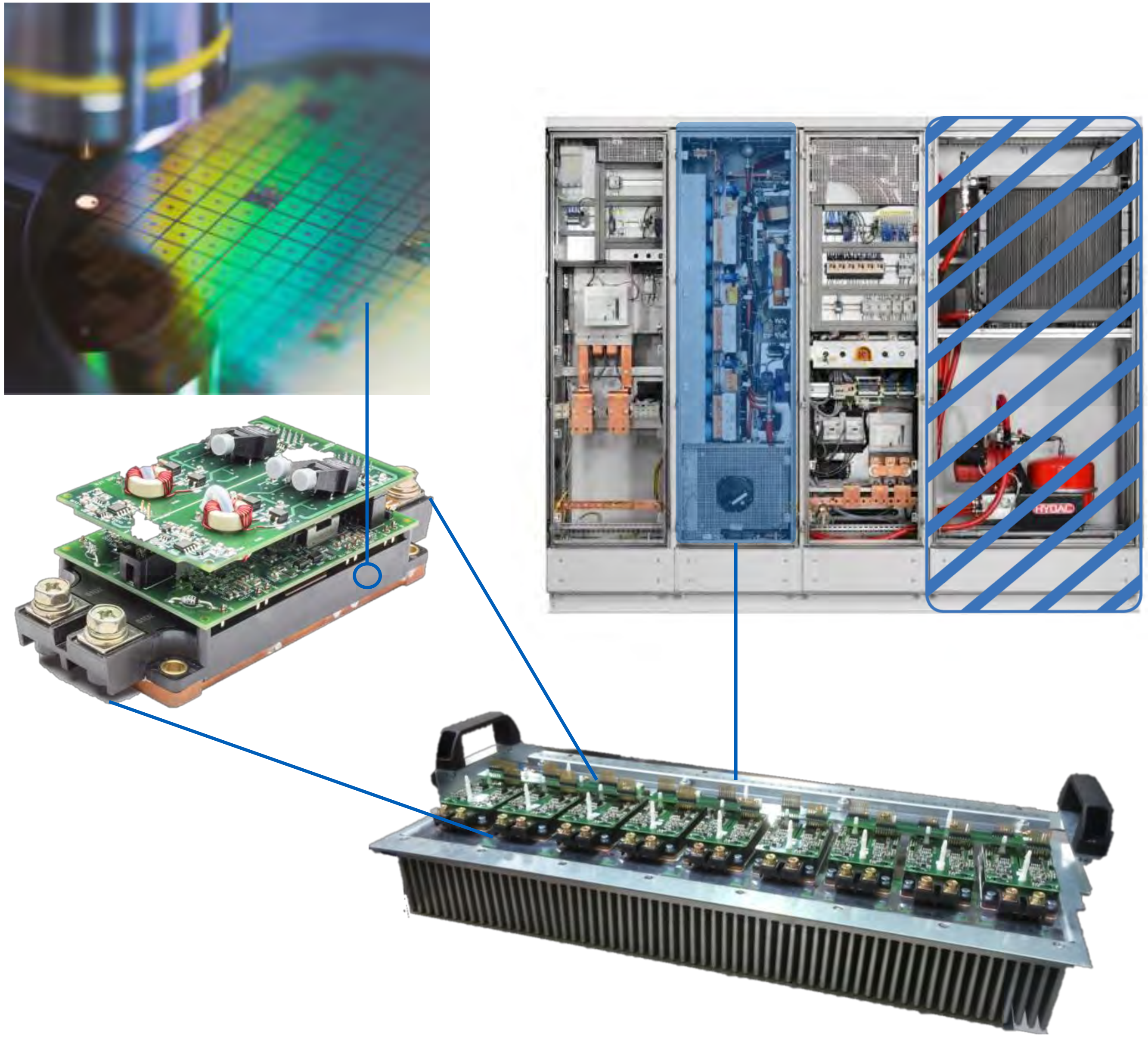
- Excellent performance
- Excellent reliability
- Very rugged

Module

- Benchmark performance: 1.7kV, 600A, 175ºC ratings
- Ultra-low Lσ for fast switching
- Advanced GDU & protection

Power Block

- Simple 2-level bridge
- High power density
- Scalable to multi-MWs
    - Perfect current sharing
    - Clean waveforms



Applications

- Higher efficiency
- Smaller footprint
- Better reliability

GE SiC advantage… vertical integration from chip to converter

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GE SiC MOSFET Chip Portfolio

Voltage	Rating @ 25°C	Chip Size	Comment (all based on 4” wafers)
1.2kV	**115mΩ, 30A**	**2.25x4.5mm²**	**1st gen, V_{gs}=20V, TO-247, 200°C, qualified per AEC-Q101**
	50mΩ, 68A	**4.5x4.5mm²**	**1st gen, V_{gs}=20V, TO-268, 200°C, qualified per AEC-Q101**
	25mΩ, 94A	**4.5x4.5mm²**	**3rd gen, V_{gs}=18-20V, TO-268, 200°C, qualified per AEC-Q101**
	54mΩ, 46A	**2.25x4.5mm²**	**3rd gen, V_{gs}=18-20V, TO-268, 200°C, qualify by similarity**
1.7kV	**29mΩ, 70A**	**4.5x4.5mm²**	**3rd gen, V_{gs}=18-20V, TO-247, 175°C, qualified per AEC-Q101**
2.5kV	45mΩ, xxA	4.5x4.5mm²	3rd gen, V_{gs}=15-18V, package TBD, 175°C in development

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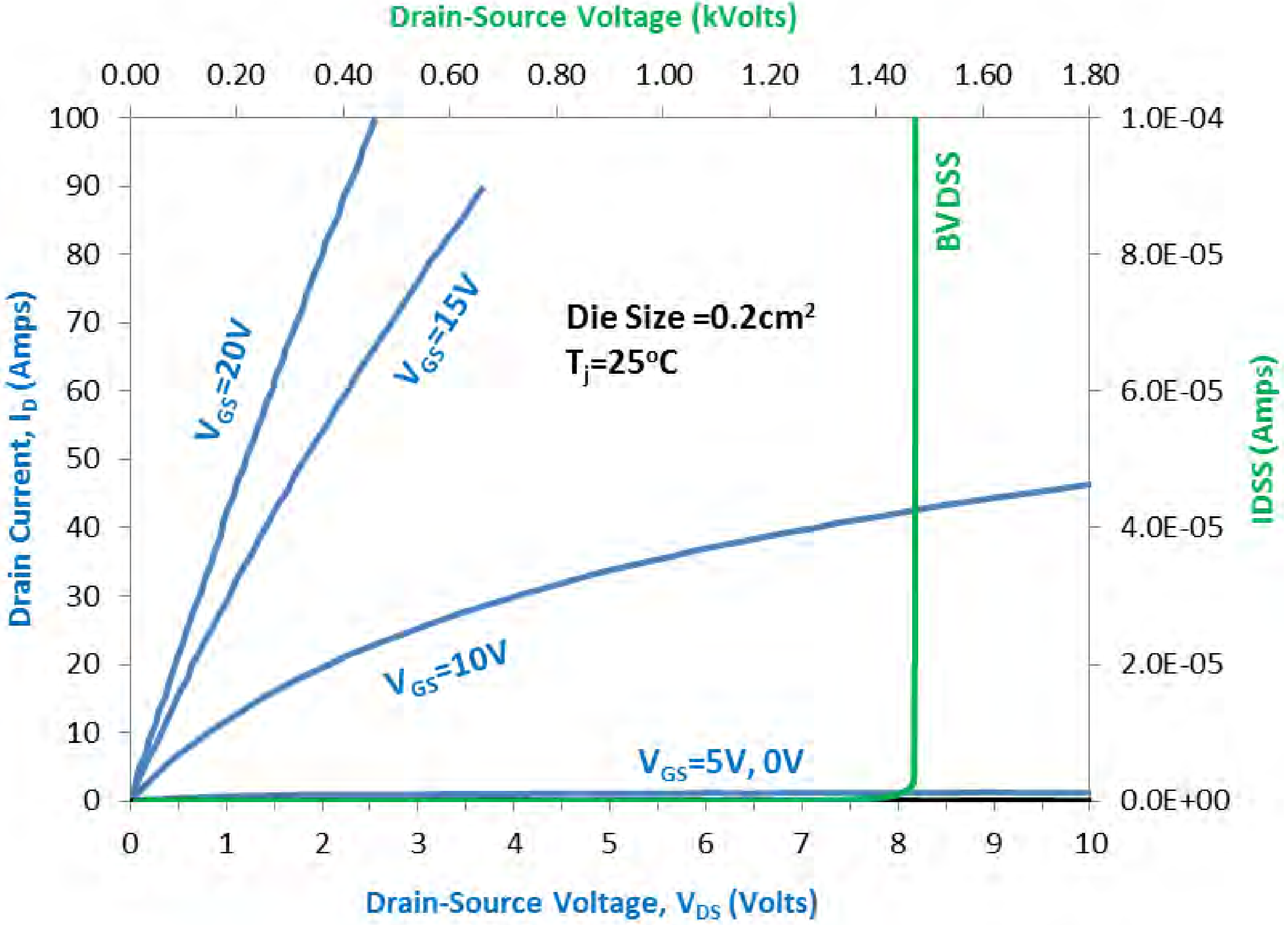
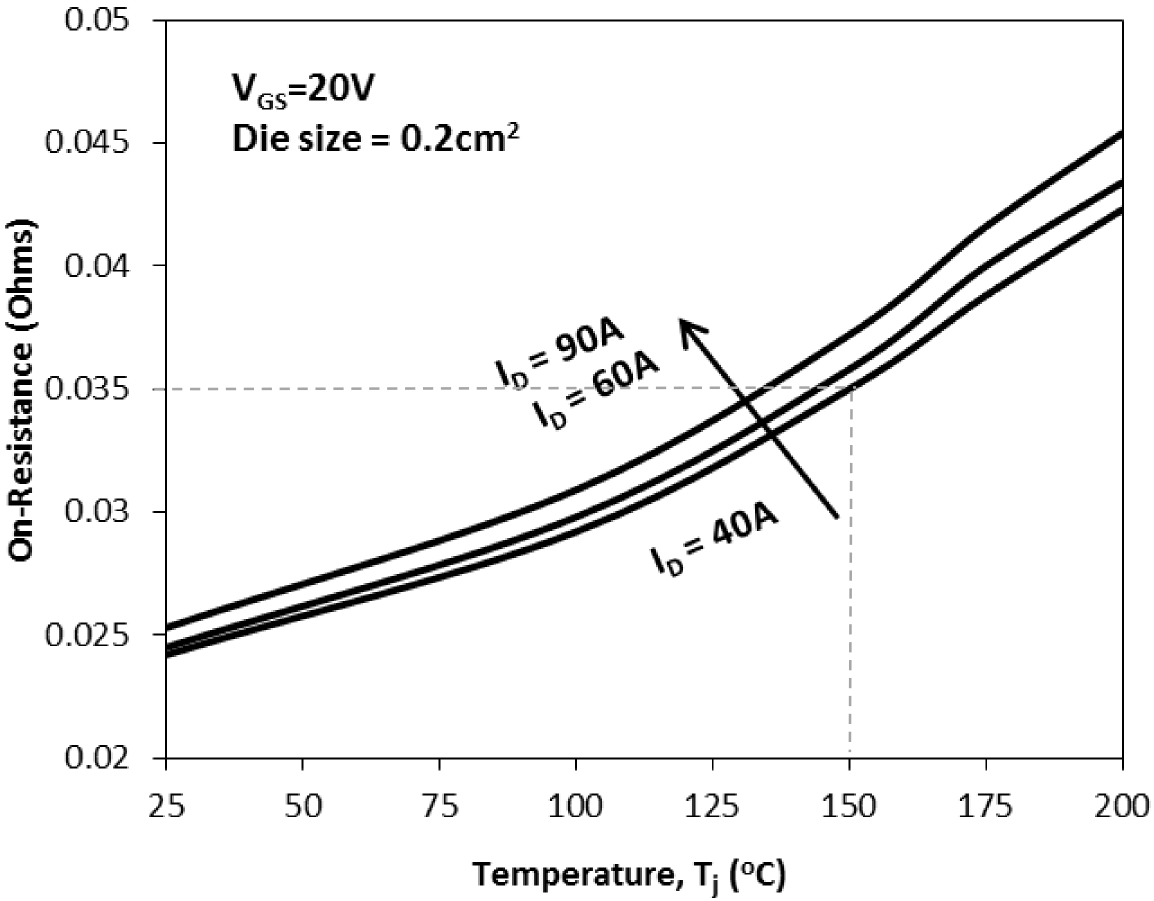
Gen-3 1.2kV MOSFET – 25mΩ, 1.2kV, 94A (@T_{CASE}=25°C)





- Die Size: 4.5mm x 4.5mm (0.2025cm²)
- 94A Rated @ T_{CASE}=25°C
- $R_{Ds,On}$=35mΩ @ T_j=150°C
- Normally off, avalanche limited BV~1.5kV

P. Losee et al., "High Performance 1.2kV-2.5kV 4H-SiC MOSFETs with Excellent Process Capability and Robustness," ICSCRM 2015

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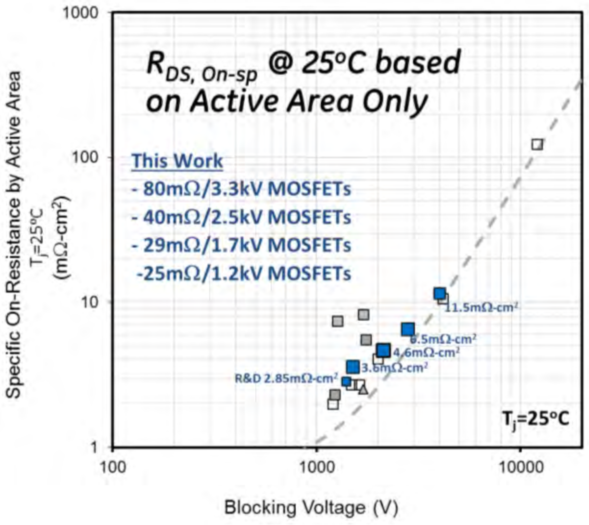
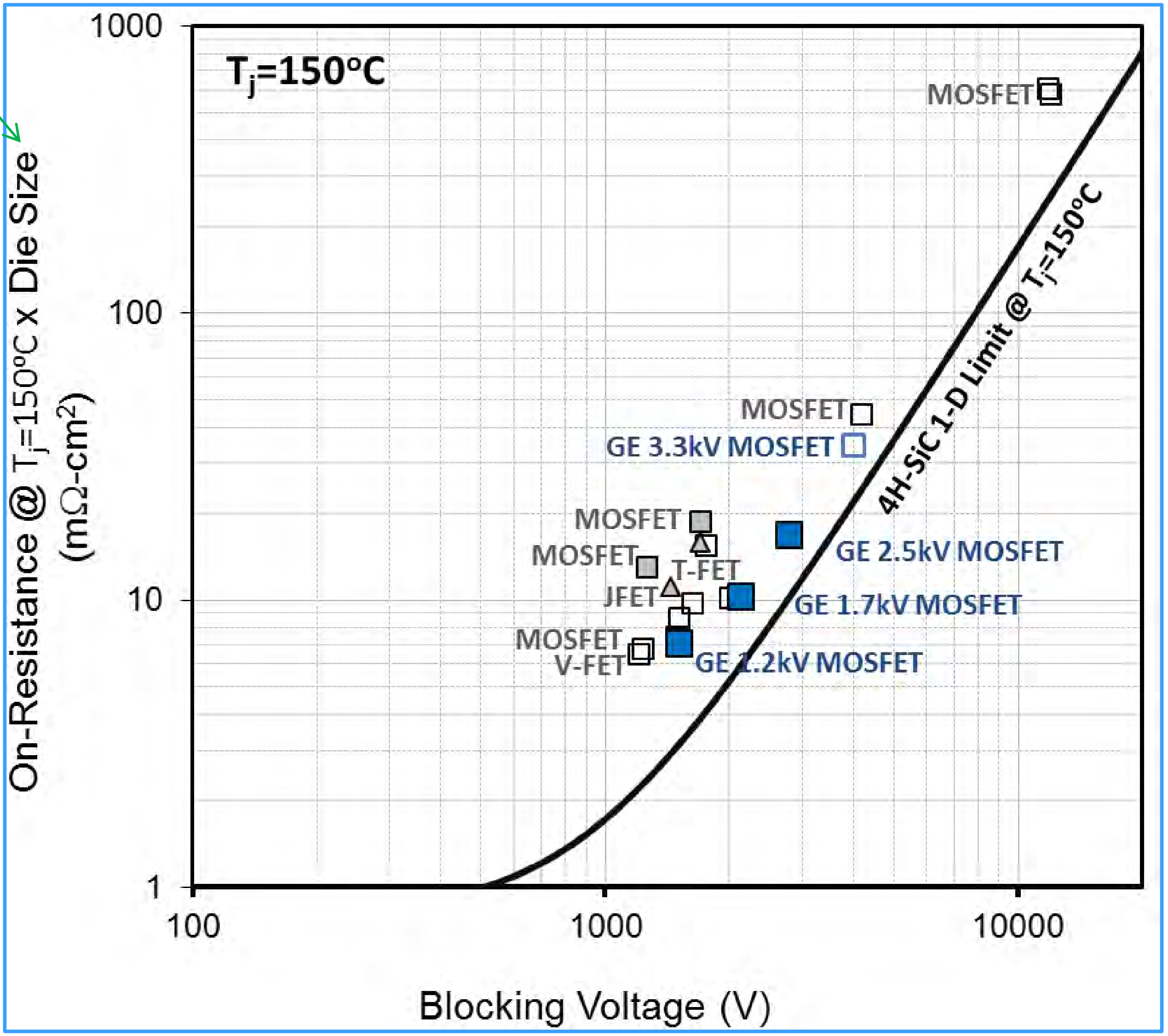
Reported Performance in SiC MOSFETs

R&D Focused Metrics



Total die area rather than just active area

Competitive Benchmarking



Continued progress in reported MOSFET performance
However, R&D benchmarking alone is not sufficient

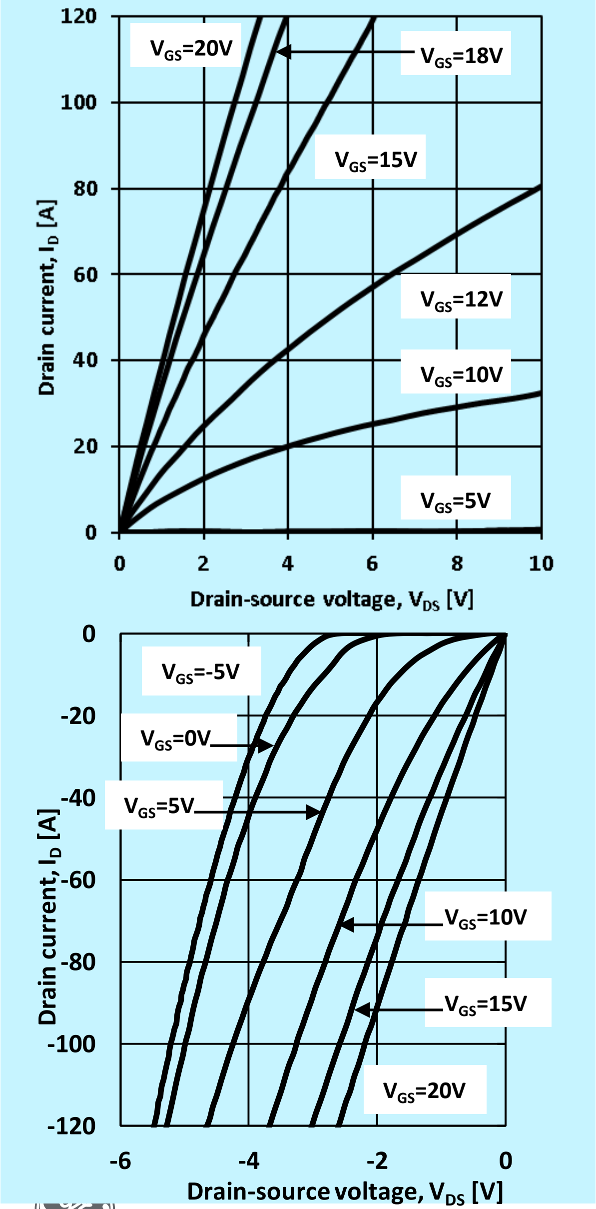
One must also consider:

- Application requirements
- Die overhead
- Manufacturability , Yield, Packaging
- Reliability, Ruggedness

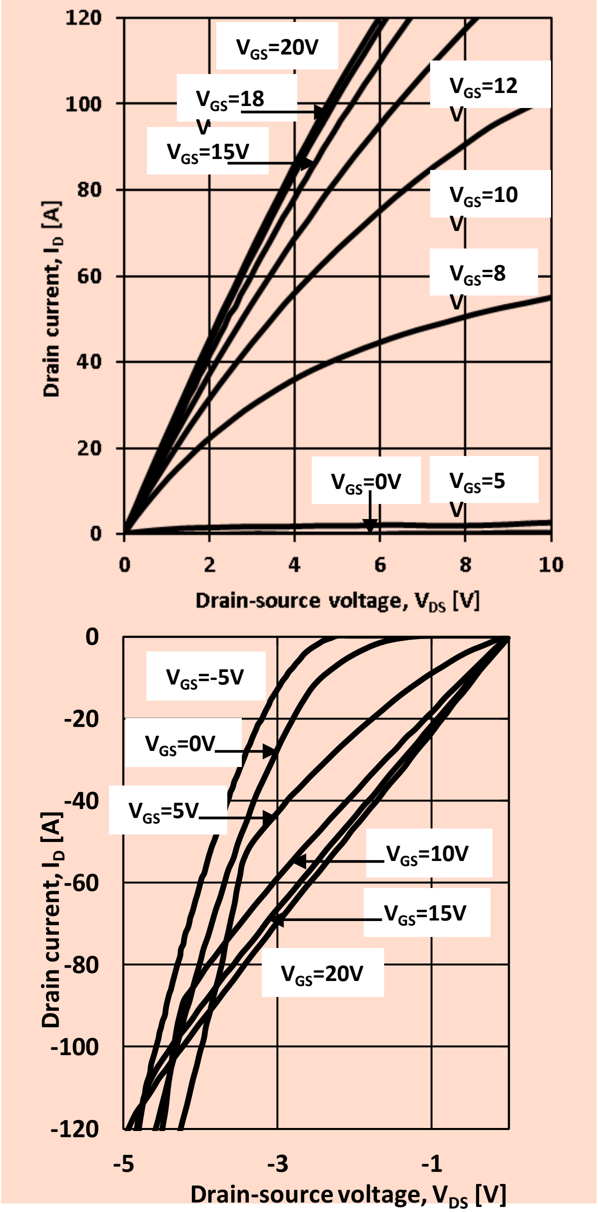
P. Losee et al., High Performance 1.2kV-2.5kV 4H-SiC MOSFETs with Excellent Process Capability and Robustness," ICSCRM 2015

1.2kV, 25mΩ MOSFET Characteristics

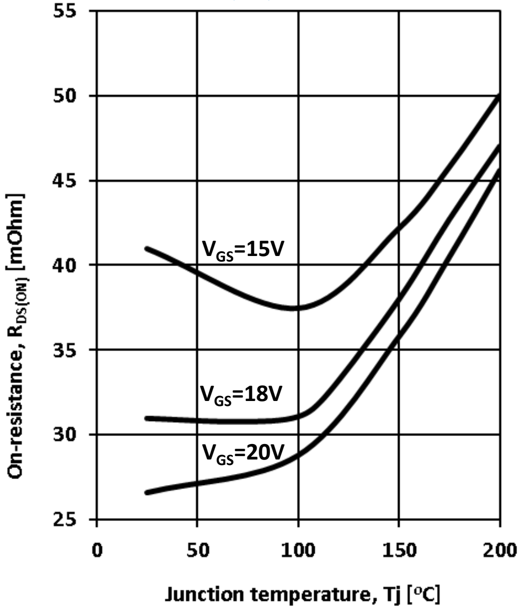
25 °C



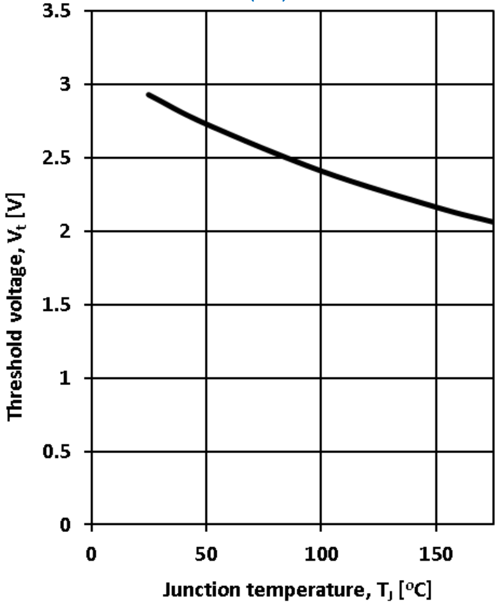
200 °C



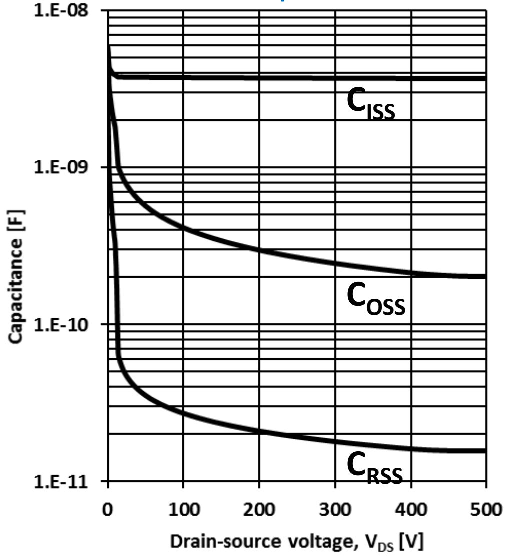
$R_{DS(on)}$ vs. T_J



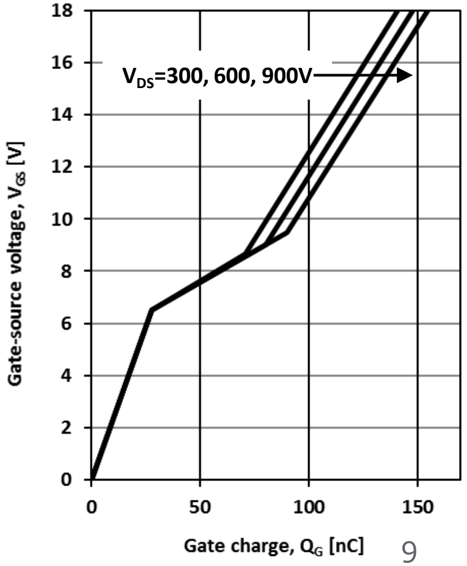
$V_{GS(th)}$ vs. T_J



Junction Capacitances



Gate Charge



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1.2kV, 25mΩ MOSFET Qual Data

94A chips, TO268 package, 200°C

Test Item	Test Condition	Test Duration	4" GRC FAB RESULTS
HTGB	Temp = 200°C, VGS = 23V	1000 Hours	1 Lots: **0 / 77**
HTRB	Temp = 200°C, VDS = 960V	1000 Hours	1 Lots: **0 / 77**
MSL1	Moisture Pre-conditioning 85°C/85% RH Level 1 Prior to TC, AC, H3TRB, IOL	168 Hours	1 Lots: **0 / 308**
Thermal Shock	-55°C to 200°C Soak: >1 min Ramp: 30°C/min ±10°C	400 Cycles	1 Lots: **0 / 77**
Autoclave	96 Hrs, 121°C, 100% Rh, 15psig	400 Cycles	1 Lots: **0 / 77**
H^3TRB	85°C, 85% RH, 100V RB	1000 Hours	1 Lot: **0 / 77**
IOL	ΔT = 100°C, 2.5 min on / 5 min off	8000 Cycles	1 Lots: **0 / 77**

Results of 1200V TO268 GE1209003B1 SiC-MOSFET Qualification

AEC-Q101 Reliability Test

Test Name	Method	Condition	n (Sample Size)	Failures
Pre- and Post- Stress Electrical test	AEC-Q101	Device Specification	597	0
External Visual	JESD22 B-101	Device Specification	597	0
Parametric Verification, Picked at Random	AEC-Q101	Device Specification	25	0
Pre-conditioning	JESD22 A-113	MSL1 Prior to TC, AC, H3TRB, IOL	308	0
High Temperature Reverse Bias (HTRB)	JESD22 A-108, MIL-STD-750-1	1000 Hrs, 200°C Tj, 960V	77	0
High Temperature Gate Bias (HTGB)	JESD22 A-108 1000 Hrs	1000 Hrs, 200°C Tj, 23V	77	0
Temperature Cycling	JESD22 A-104	400 Cycles, TC -55 to 200C	77	0
TC Delamination Test	JESD22 A-104, J-STD-035	CSAM Post TC	77	0
Autoclave	JESD22 A-102	96 Hrs, 121°C, 100% Rh, 15psig	77	0
High Humidity, High Temperature Re-verse Bias (H3TRB)	JESD22 A-101	1000 Hrs, 85°C/85% RH, 100V	77	0
Intermittent Operational Life (IOL)	MIL-STD-750 Meth-od 1037	100°C Δ Tj	77	0
ESD Characterization (CDM,HBM,MM)	AEC-Q101	001, 002, 005	90	H2, M4, C5
Destructive Physical Analysis	AEC-Q101-004	POST TC, H3TRB, IOL	9	0
Physical Dimension	JESD22 B-100	Device Specification	10	0
Solderability	J-STD-002	Eutectic SnPb, 235°C	10	0
Thermal Resistance	JESD24-3	Device Specification	10	0
Wire Bond Strength	MIL-STD-750 Meth-od 2037	Min. 28g Gate, Min. 130g Source	5	0
Bond Shear	AEC-Q101 -003	Min. Tensile Strength of Wire	5	0
Die Shear	MIL-STD-750 Meth-od 2017	Min. 5kG	5	0
Unclamped Inductive Switching	AEC-Q101-004 Sec-tion 2	Device Specification	5	0
Dielectric Integrity	AEC-Q101-004 Sec-tion 3	Device Specification	5	0

...

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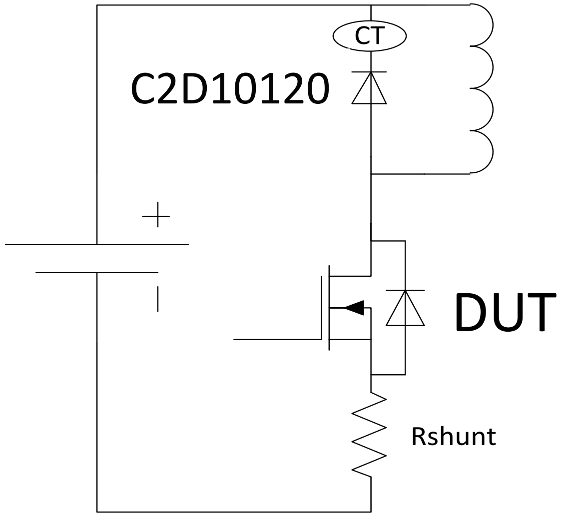
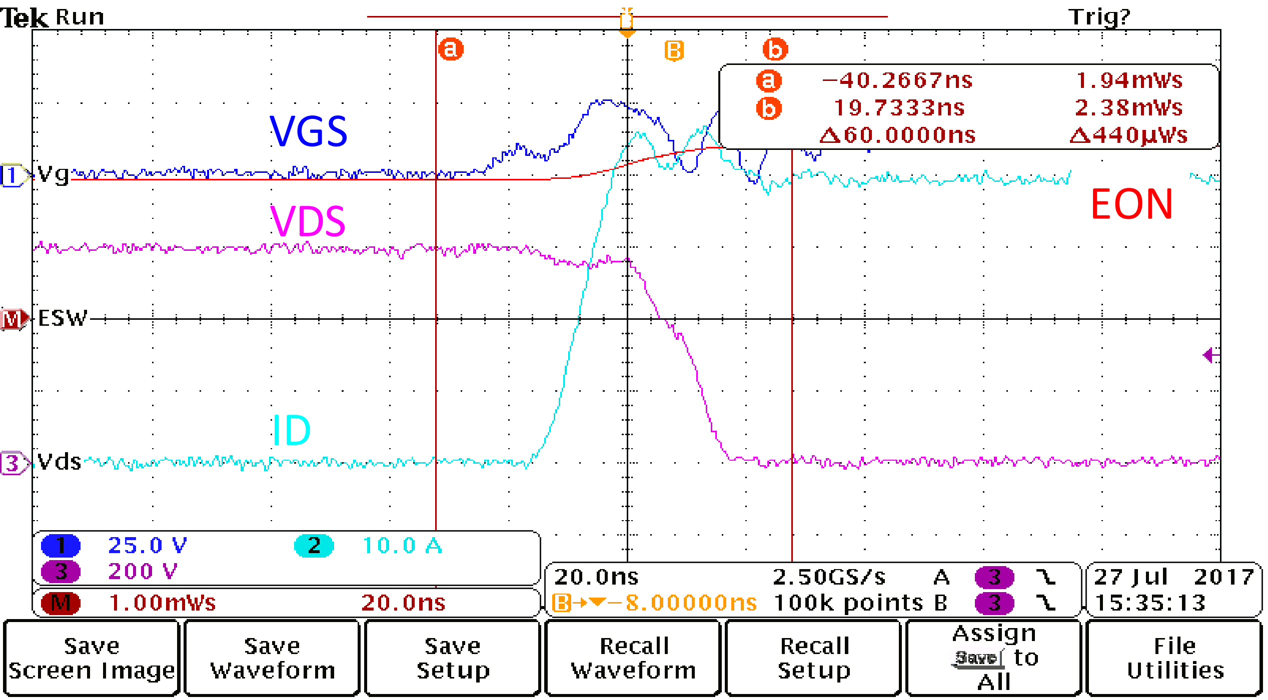
1.2kV MOSFET Switching Losses

Double-pulse Inductive Switching, T=25ºC

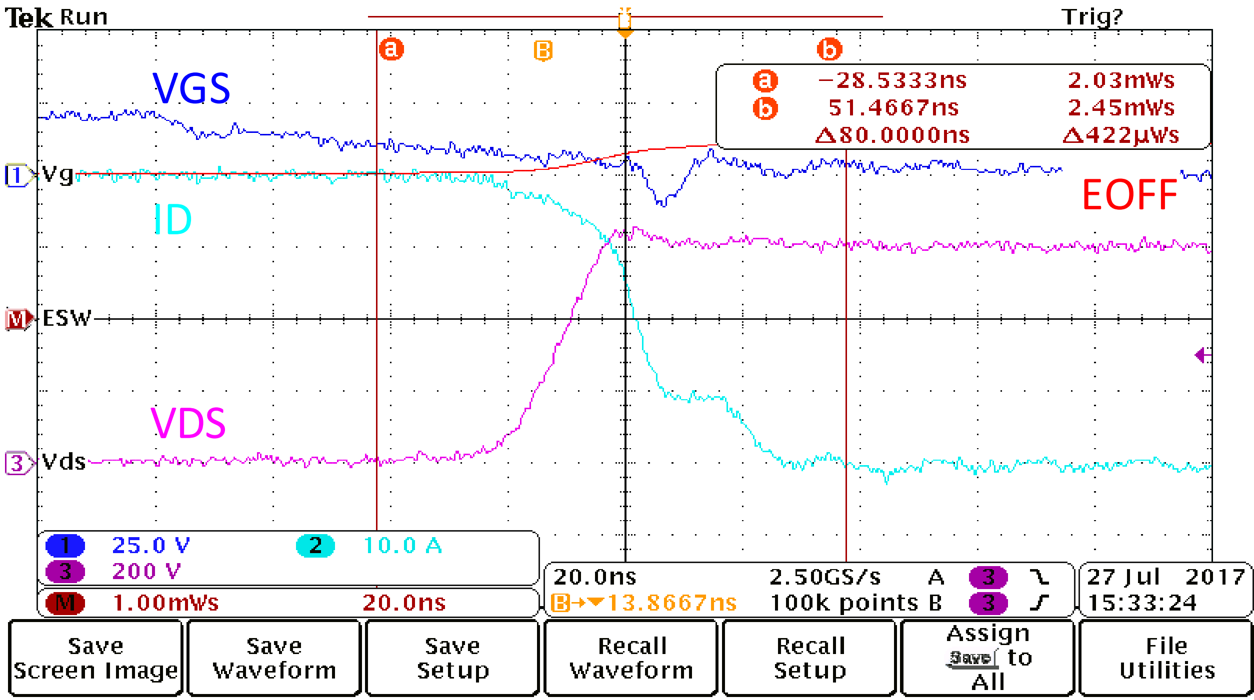
V_{DS} = 600 V,
I_D = 40 A,
V_{GS} = 0 / 20 V,
R_G = 5.6 Ω,
L = 4.5 mH,
FWD = C2D10120



Turn-on:



Turn-off:



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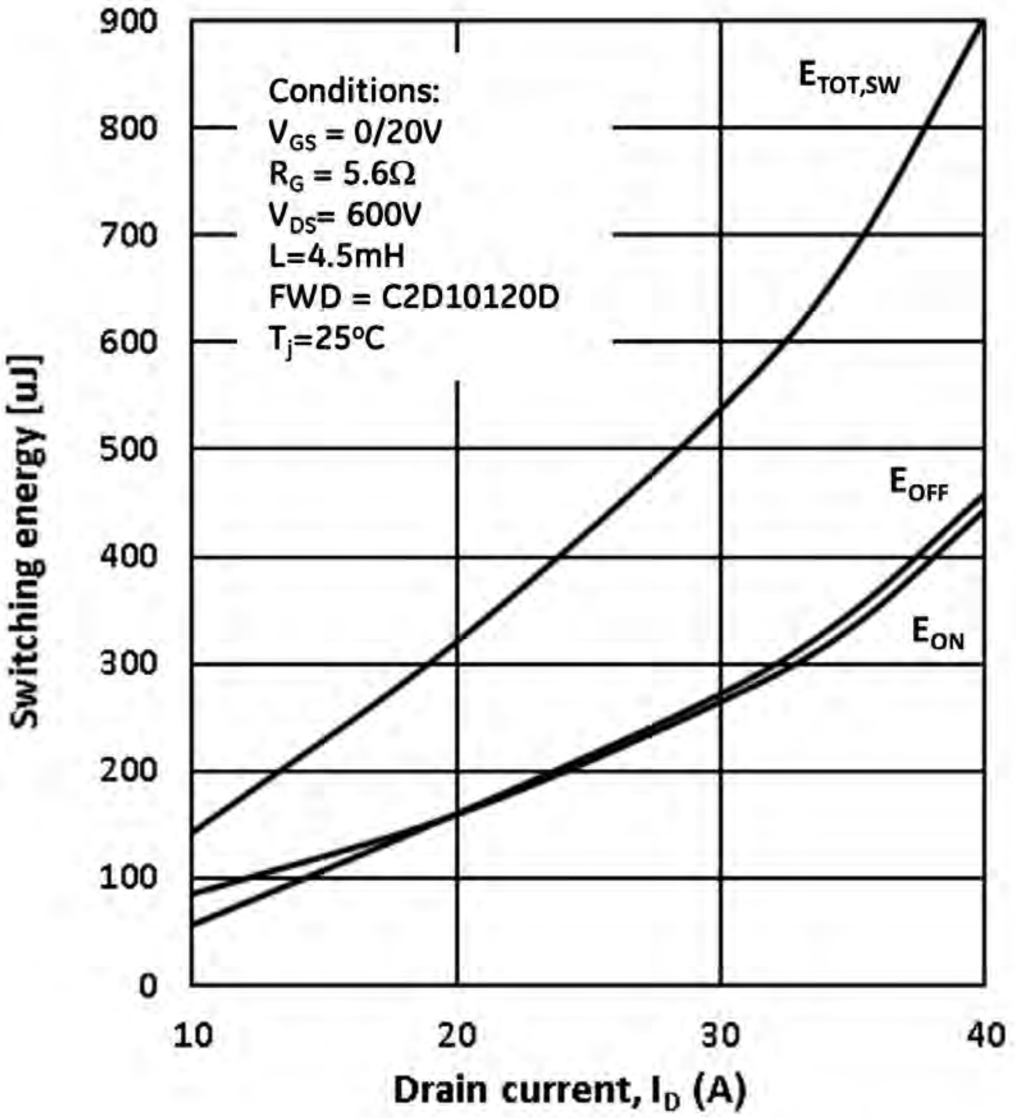
1.2kV MOSFET Switching Losses, Summary

Double-pulse Inductive Switching, T=25^oC



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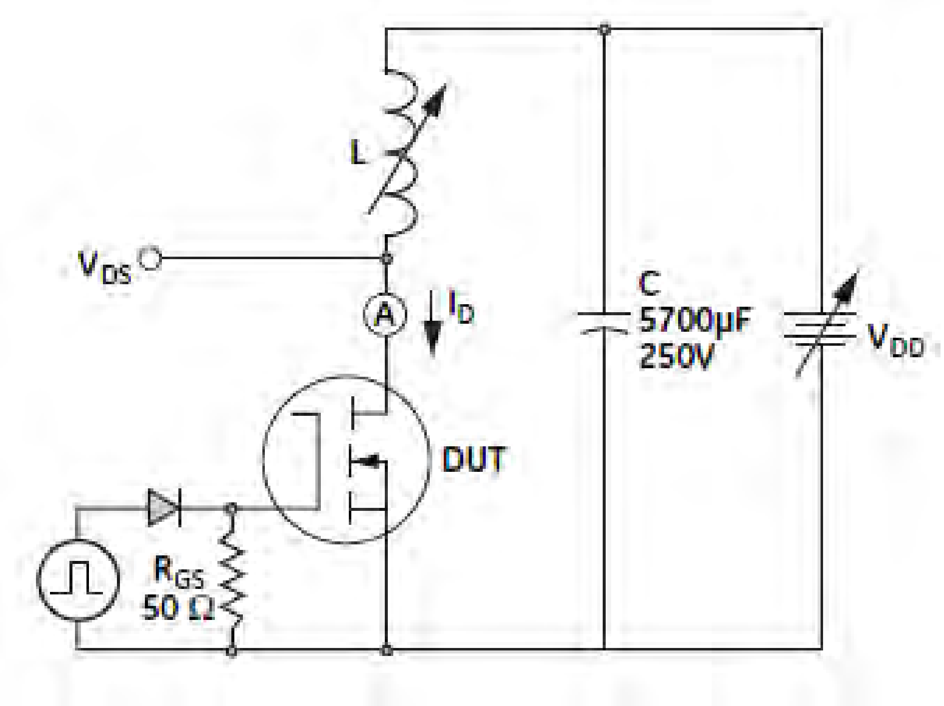
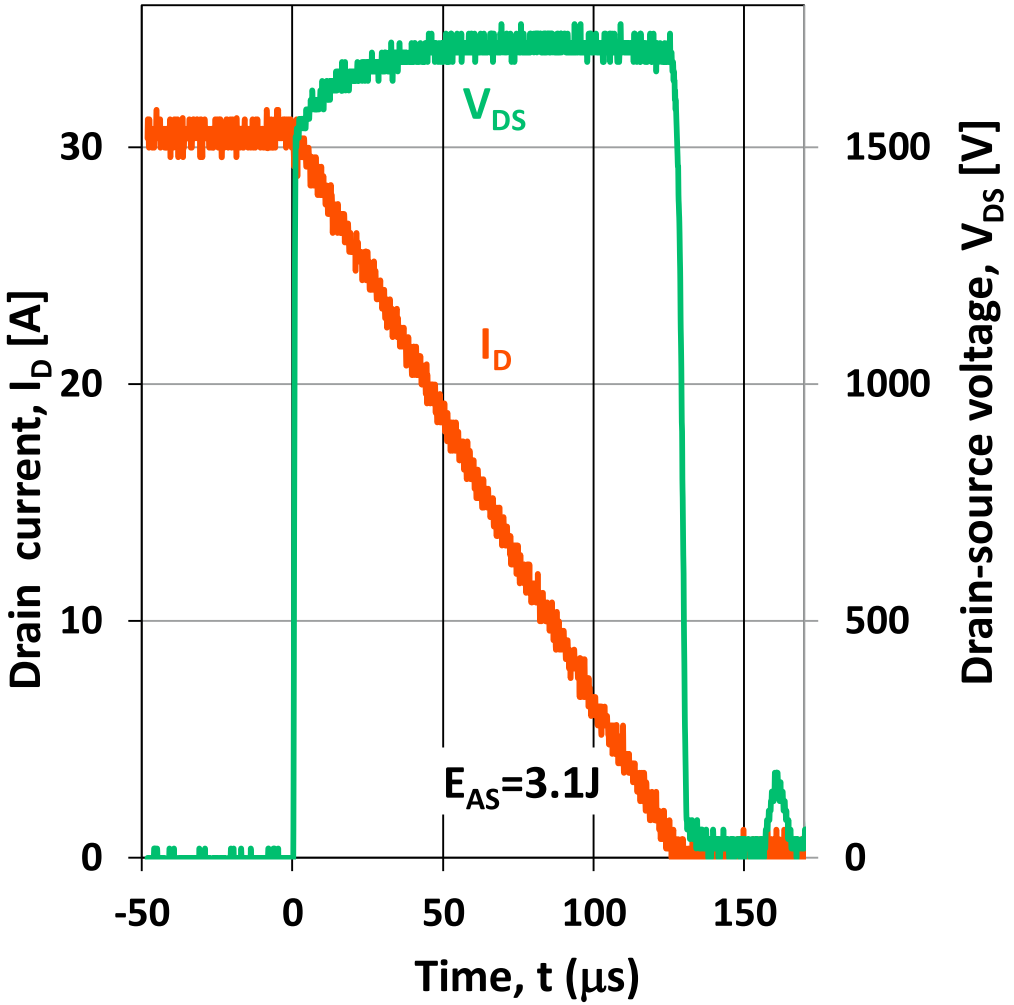
1.2kV MOSFET - Avalanche Ruggedness

Unclamped Inductive Switching (UIS)





- 1.2kV, 94A SiC MOSFET: E_{AV} >8J/cm^2
- Robust design-process results in good uniformity

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1.2kV MOSFET - Avalanche Energy Uniformity & Scaling

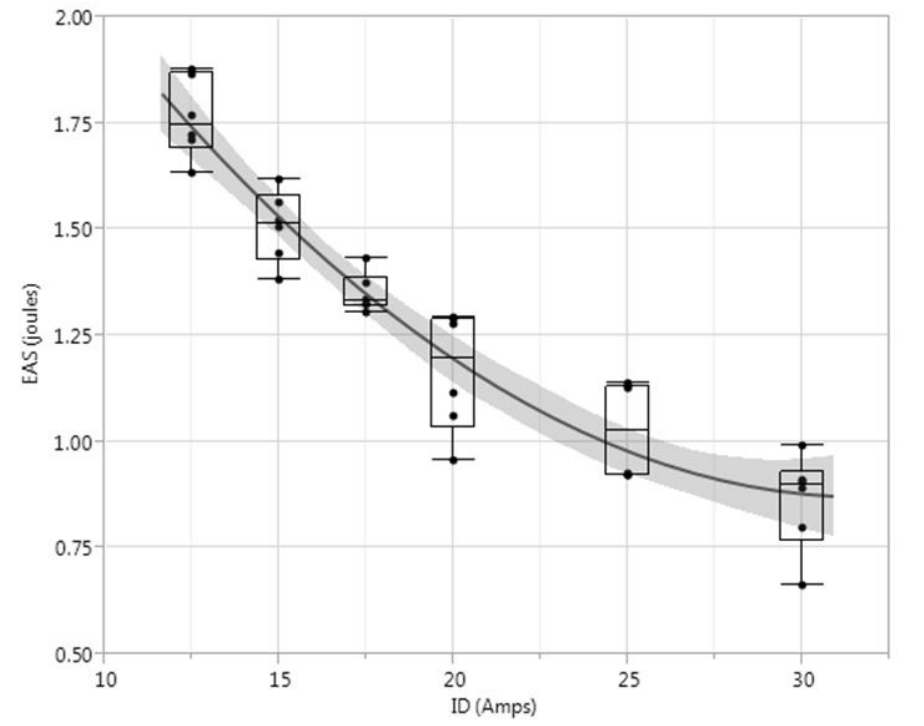


Figure 16. Single-Pulse Avalanche Energy (E_{AS}) versus Drain current (I_D) for A=0.1cm^2, 1.2kV SiC MOSFETs, N=36pcs

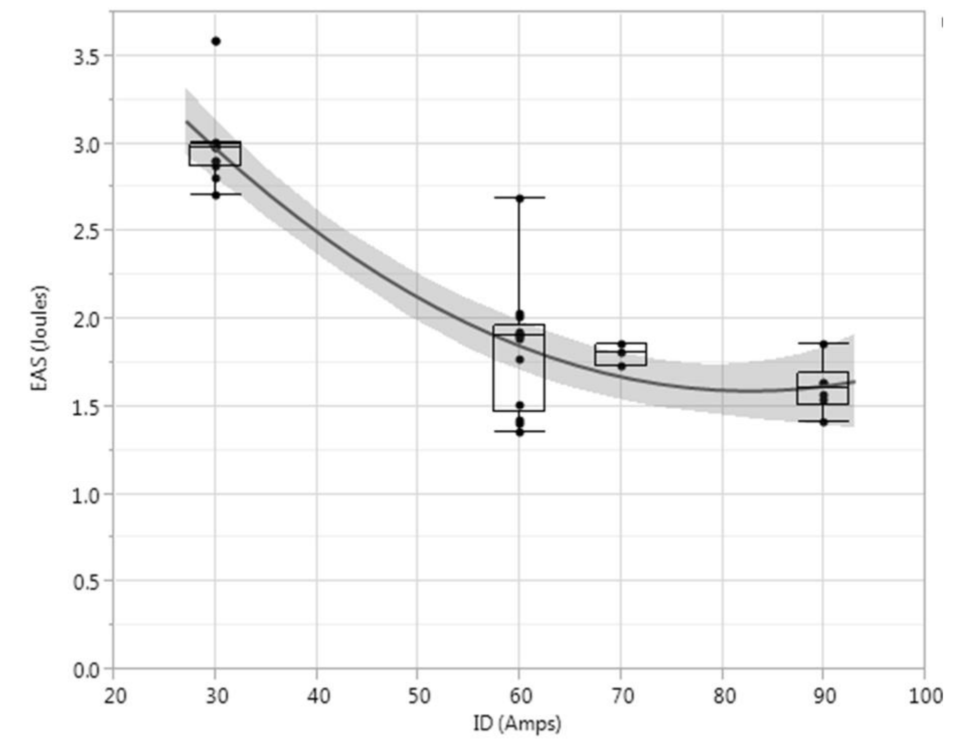


Figure 17. Single-Pulse Avalanche Energy (E_{AS}) versus Drain current (I_D) for A=0.2cm^2, 1.2kV SiC MOSFETs, N=34pcs

- Good scaling between avalanche energy $E_{AV\_TO\_FAILURE}$ and die size
- Repeatable distribution across lot/wafer
- Failures randomly scattered around active area

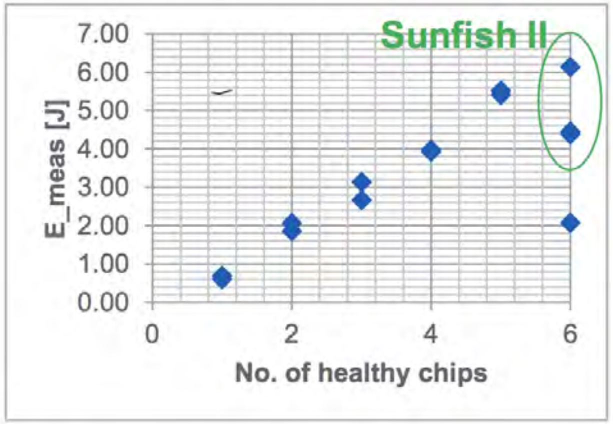
	2.25x4.5mm Die	4.5x4.5mm Die	
J_D (A/cm^2)	Mean E_{AS} Density (J/cm^2)	Mean E_{AS} Density (J/cm^2)	Difference
148	15.1	14.7	2.9%
198	11.9	12.3*	4.2%
296	8.7	9.1	5.1%

P. Losee et al., "SiC MOSFET Design Considerations for Reliable High Voltage Operation," invited talk at IEEE IRPS 2017

Pre-emptive N+1 Mode

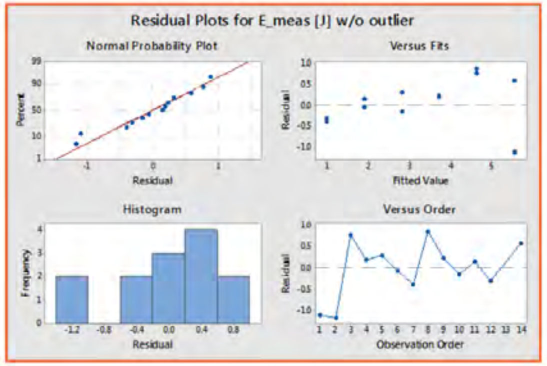
Self-Clamping Experimental Results (2)

1. Self-clamping Experiment



- MOSFET begins self-clamping at ~2 kV overvoltage.
- Single chip fails short @ overvoltage
  → Feature enables Reactive N+1 Mode

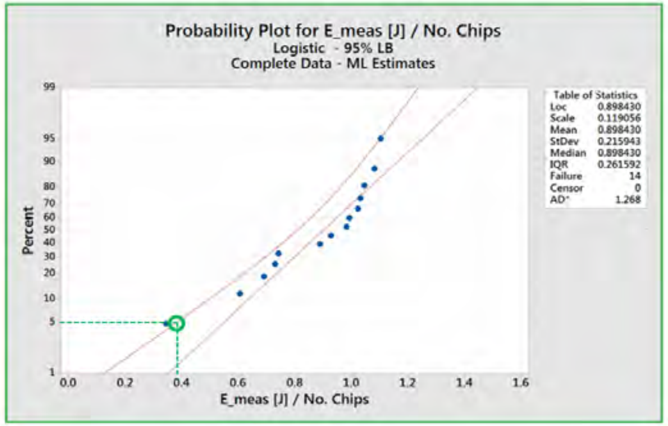
2. Regression Analysis



E_meas [J] w/o outlier = 0.085 + 0.911 No. healthy chips [n]

Self-clamping energy causing breakdown of single chip.
→ linear w/ no. of healthy chips.

3. Clamping Capability Estimation



With 95% confidence, the average self-clamping energy at which 5% of the MOSFET chips fail is not lower than **0.38 J.**

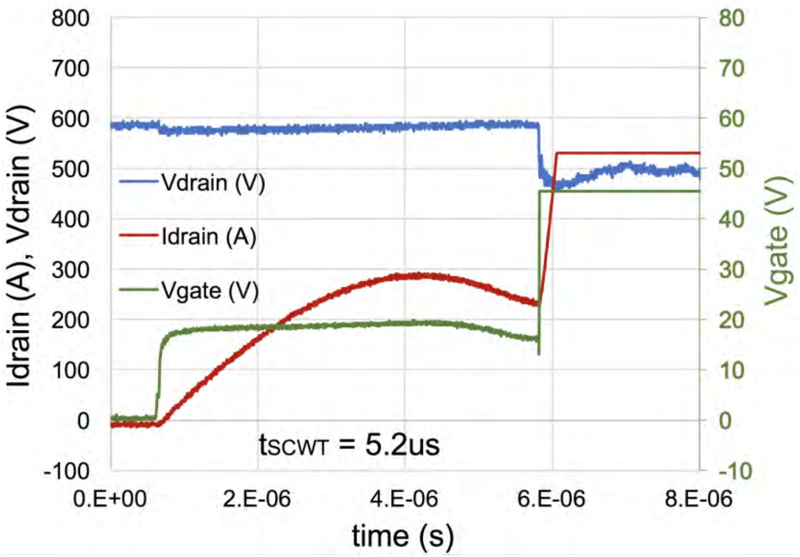
SiC MOSFET self-clamping capability expected to be **> 4 us** at load current for Sunfish III module.

SiC Module	E_clamp, expect	I_clamp, max	t_clamp, min
Sunfish II	2.28 J	340 A	3.35 µs
Sunfish III	4.56 J	566 A	4.03 µs

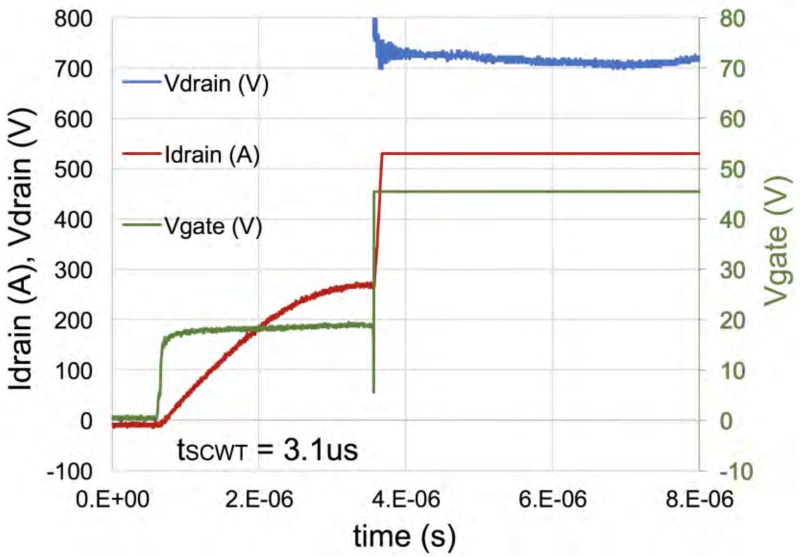
1.2kV, 25mOhm MOSFET - Short Circuit Withstand Time

- Short Circuit Withstand Time (SCWT) capability important for system safety
- Converter controls typically require $t_{SCWT} \geq$10us for fault detection and shut-down
- Below are typical SCWT test results for the Gen-3 GE MOSFETs (GE1209003B1):

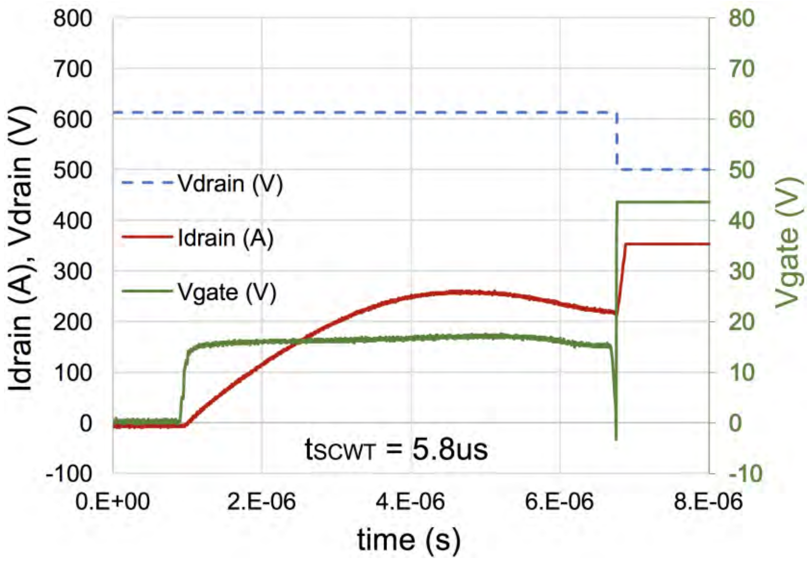
V_{DS} = 600V, V_{GS} = 20V



V_{DS} = 960V, V_{GS} = 20V



V_{DS} = 615V, V_{GS} = 18V



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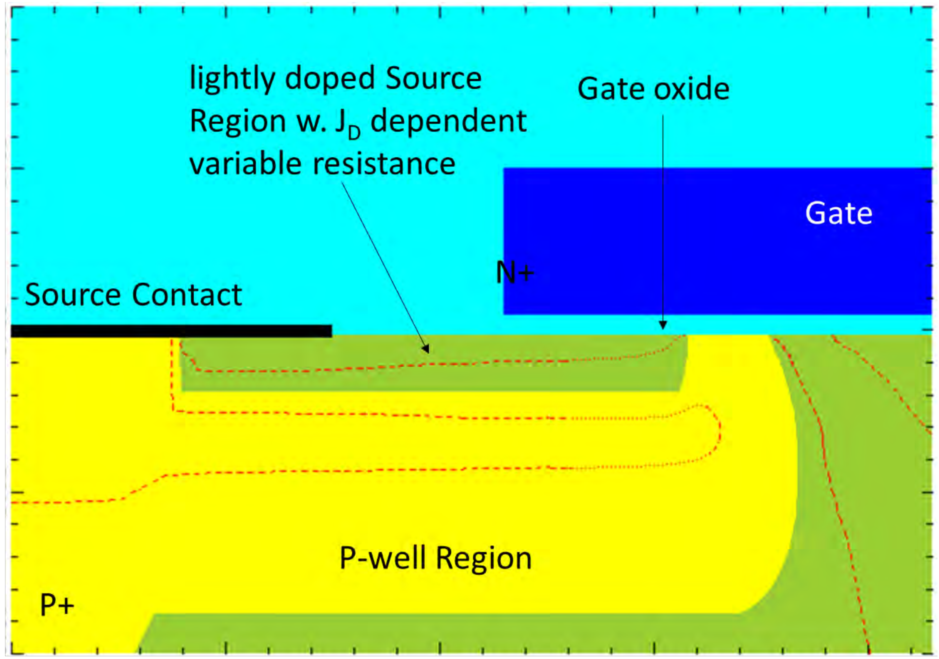
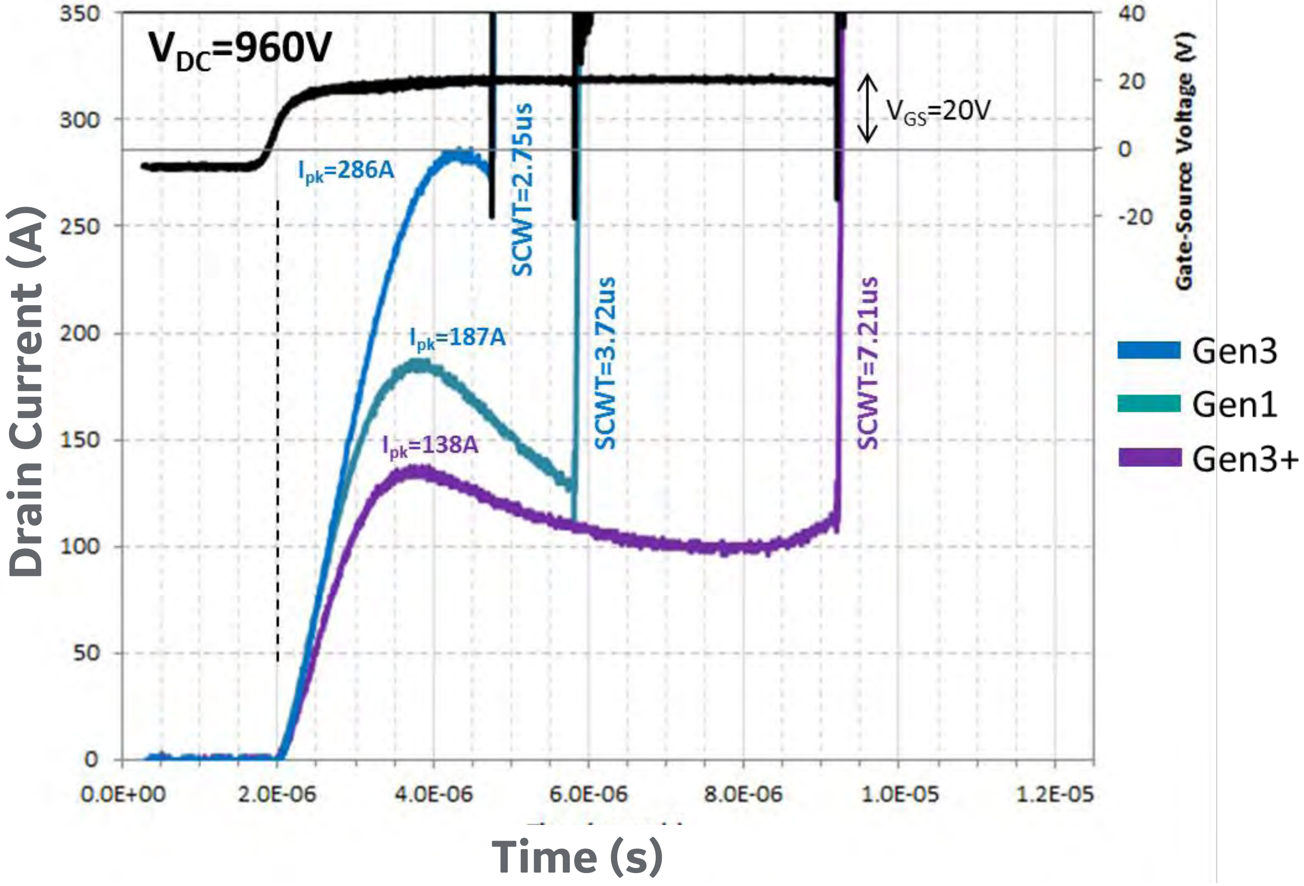
Gen-3+ GE MOSFET: Fault Current Self-limiting

- Short Circuit Withstand Time important for safety
- Gen-3 MOSFETs optimized for lowest $R_{DS,ON}$ with SCWT of ~3us, vs. ~10us for Si IGBTs
- Coping strategy: GDU with fast controls to detect and defuse SC faults in <1us
- Optimize R_{ON} vs. SCWT tradeoff, differentiate w/ Fault Current Self-limiting (FCS)
- Type-1 SC target: SCWT > 5us @ 960V, 125°C



N-type Drift Region, N+ substrate, Drain Contact ↓

Type-1 SC test results for 1.2kV GE MOSFETs, V_{DC}=960V_{DC}



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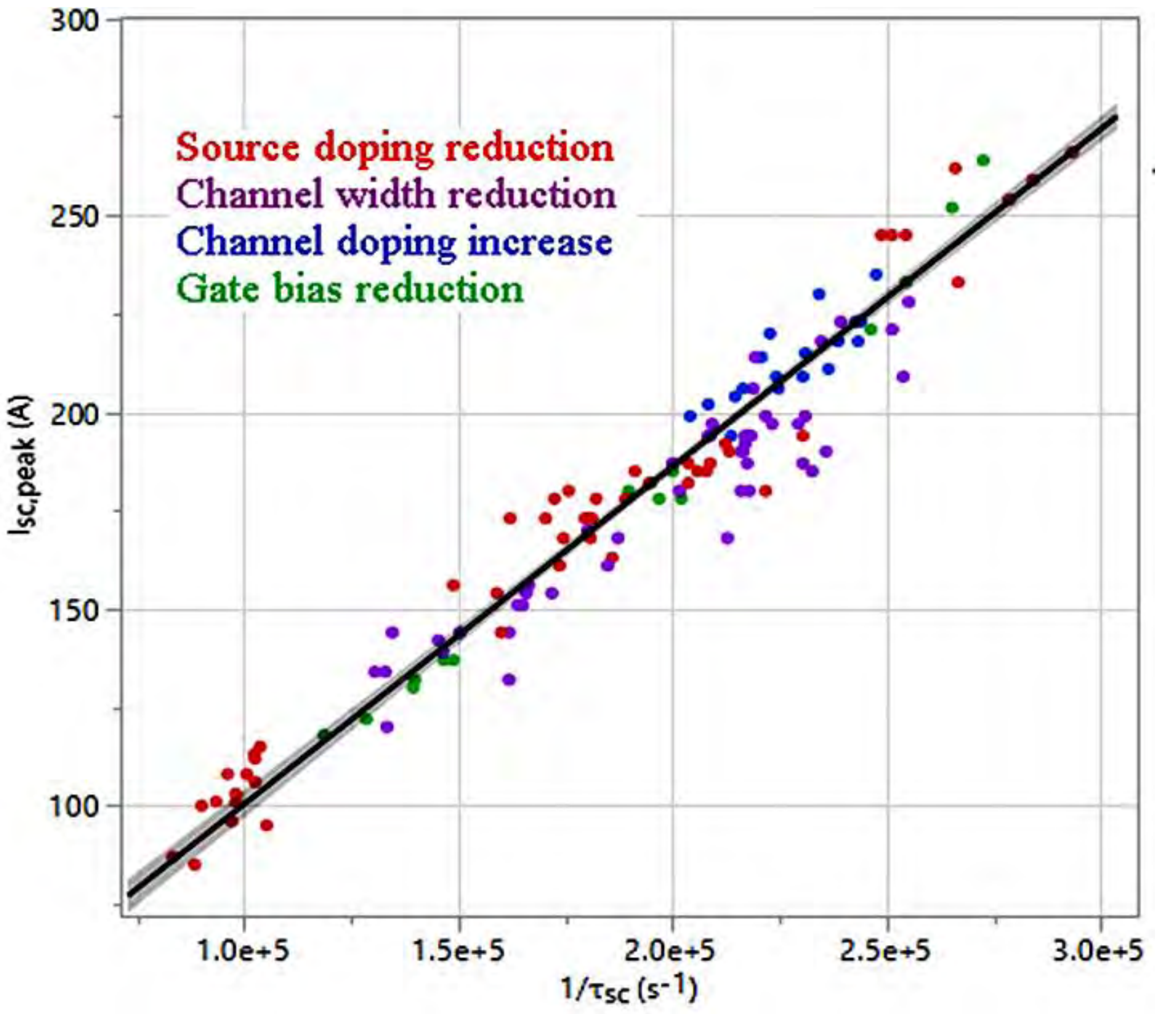
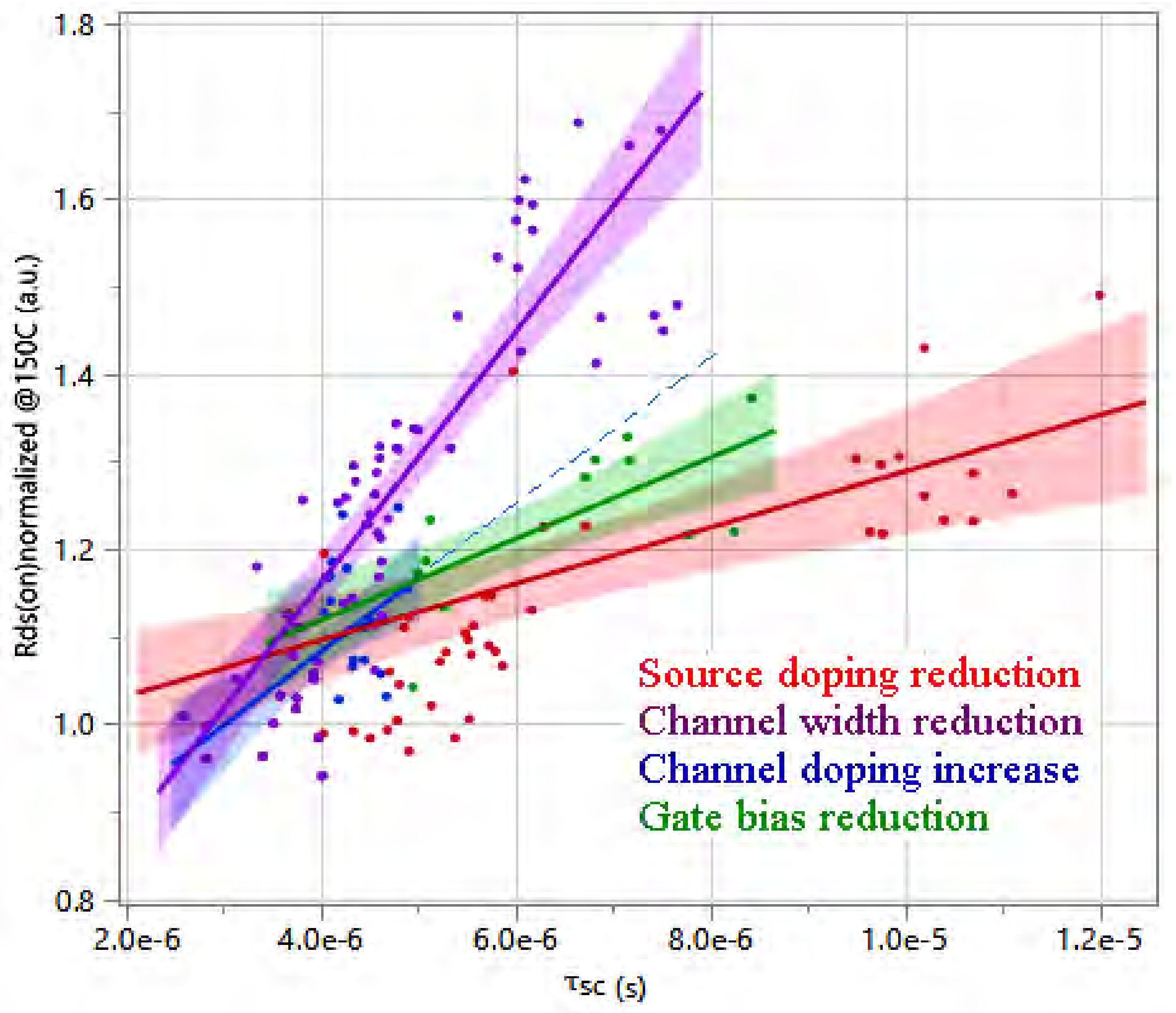
1.7kV, 30A G3 MOSFET Short Circuit Performance, Test Results

Peak current vs. SCWT for different approaches



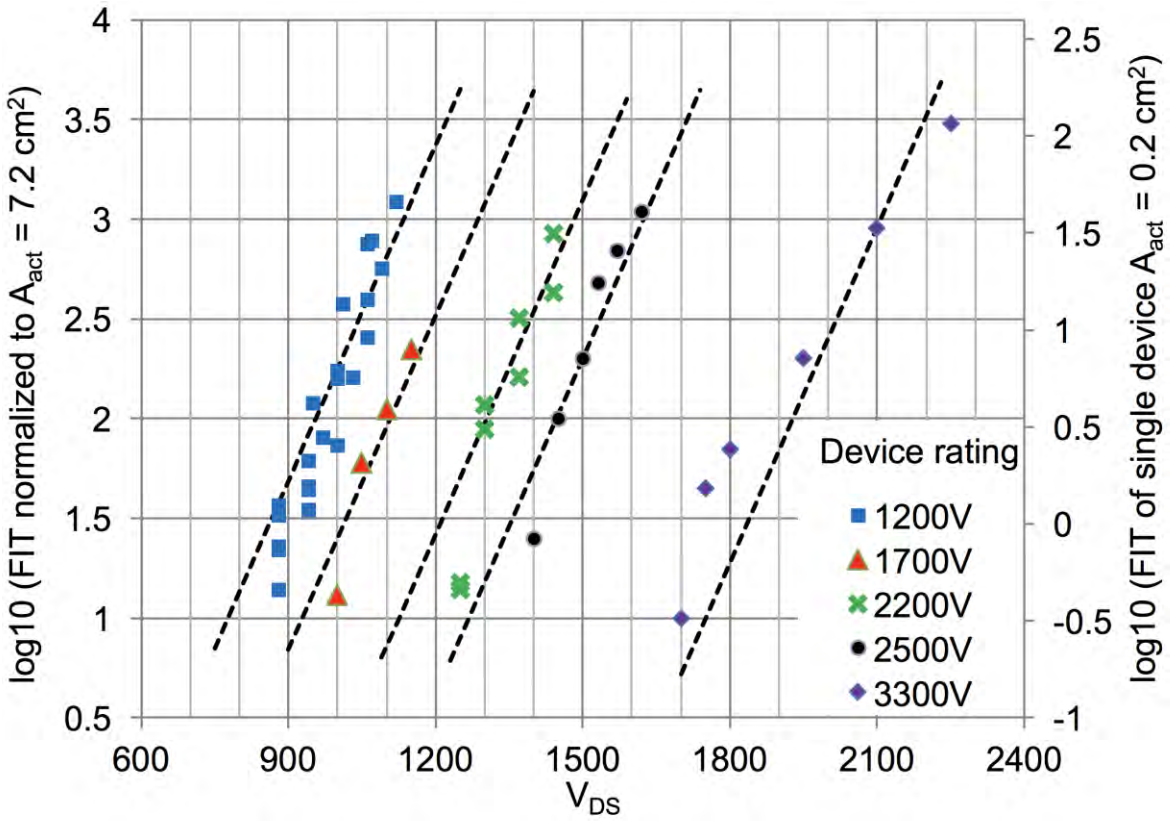
$R_{DS,ON}$ vs. SCWT trade-off summary for different approaches

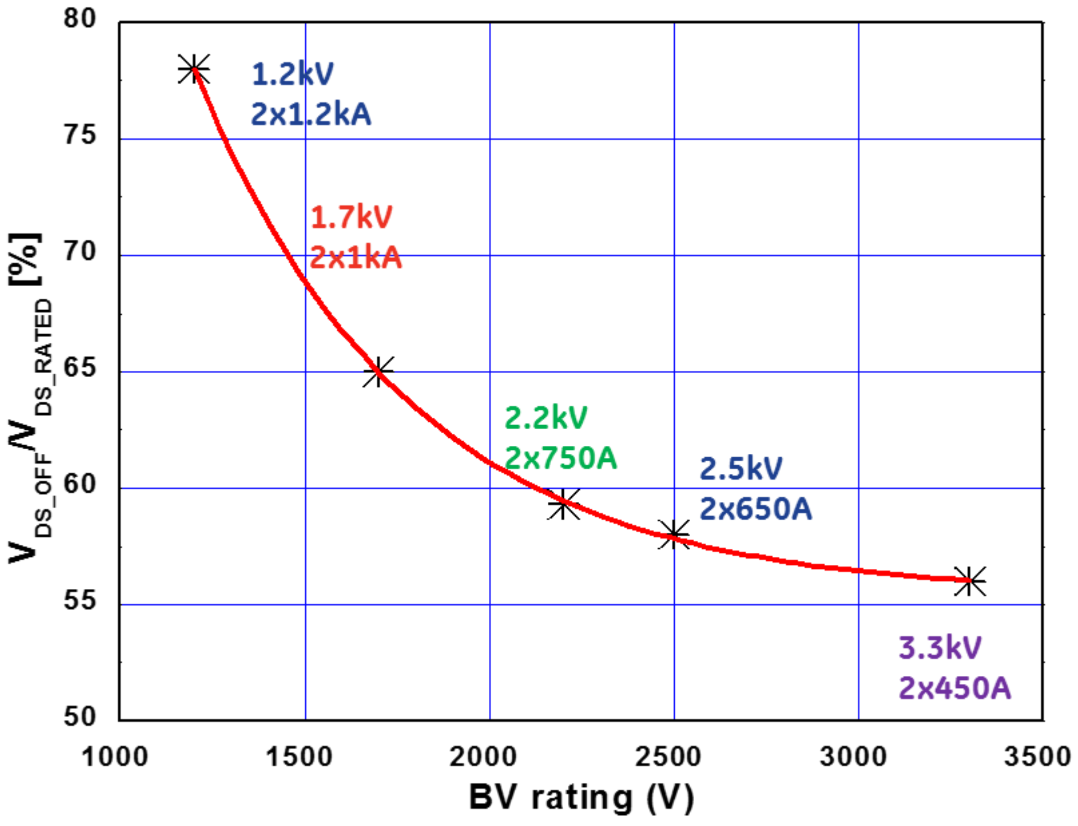


A. Bolotnikov, "Optimization of 1700V SiC MOSFET for Short Circuit Ruggedness," to be presented at ECSCRM2017

GE SiC MOSFET Terrestrial Cosmic Radiation FIT Rate

Experimental results at room temperature, sea level





Total MOSFET active area of A_{act} =7.2cm^2 corresponds to the following module ratings:
2x1.2kA for 1.2kV; 2x1.0kA for 1.7kV; 2x750A for 2.2kV; 2x650A for 2.5kV; 2x450A for 3.3kV
(2x denotes dual, or half-bridge module configuration)

A. Bolotnikov et al., “Overview of 1.2kV – 2.2kV SiC MOSFETs targeted for industrial power conversion applications” 2015 APEC

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GE SiC MOSFET Module

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SiC MOSFET Dual Modules

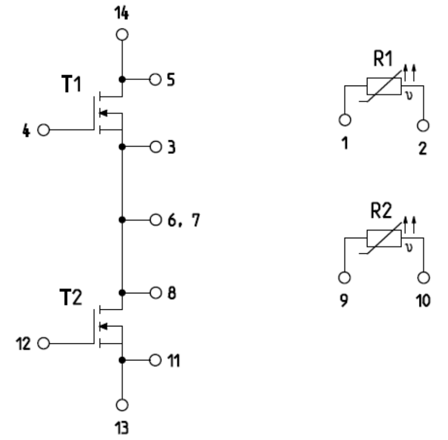
Voltage	Rating @ 100°C	Module type
1.2kV	2.3 mΩ, 650 A	Dual, 12 die/switch
1.7kV	2.6 mΩ, 550 A	Dual, 12 die/switch
2.5kV	TBD mΩ, xx A	Dual, TBD die/switch

1700 V SiC Power Module

GE Silicon Carbide MOSFET half-bridge module offers superior performance for high power, high frequency applications.

Features:

- Low $R_{DS(on)}$ (2.6 mΩ @ RT & V_{GS} = 20 V, measured from power terminals)
- Low inductance for fast switching
- Low, temperature invariant switching losses
- Body diode with low reverse recovery losses
- Low thermal resistance: R_{thJC} = 48 ^{o}C/kW



Applications:

- PV inverters, wind converters, UPS
- Motor drives, traction inverters
- MRI amplifiers, HF converters, induction heating

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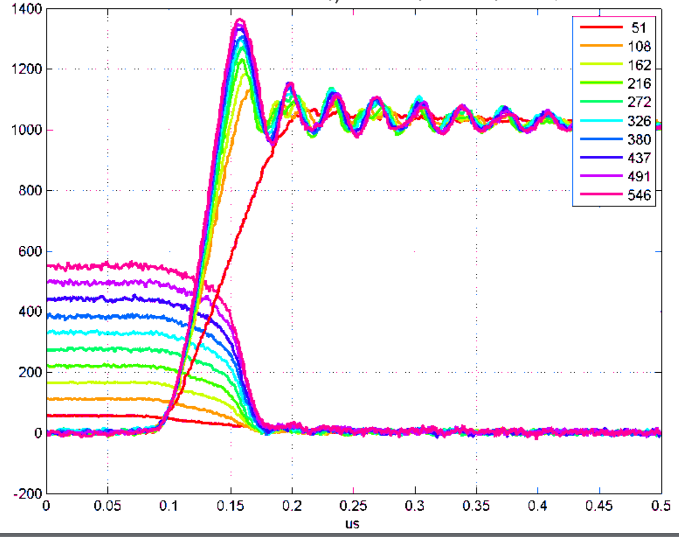
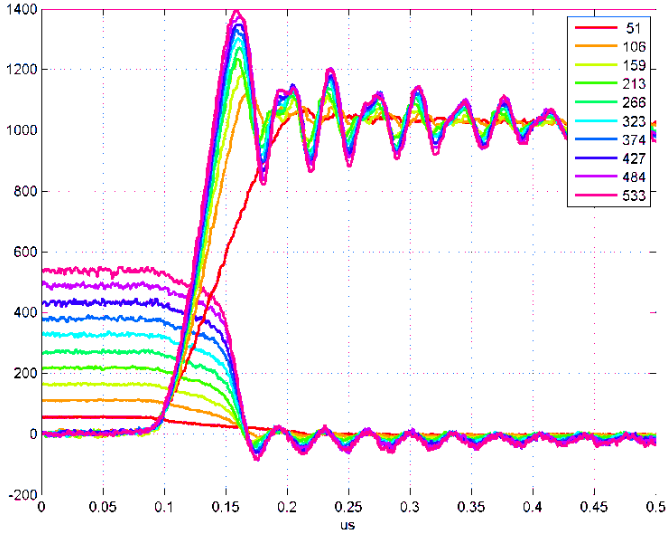
Multi-plots as Function of Load Current

Turn off @ 150°C, 1000V

51A - 546A, lower device

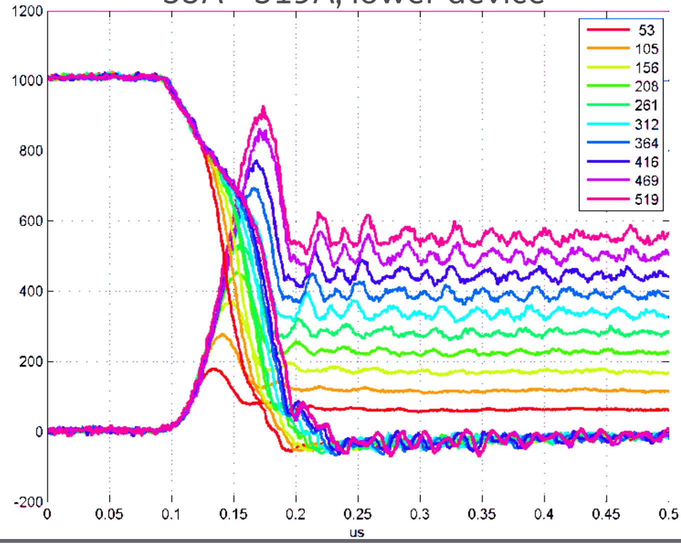


51A - 533A, upper device

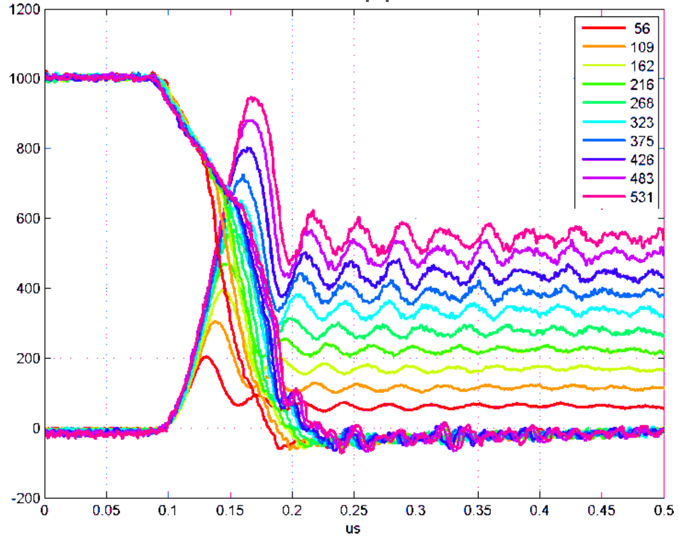


Turn on @ 150°C, 1000V

53A - 519A, lower device



56A - 531A, upper device



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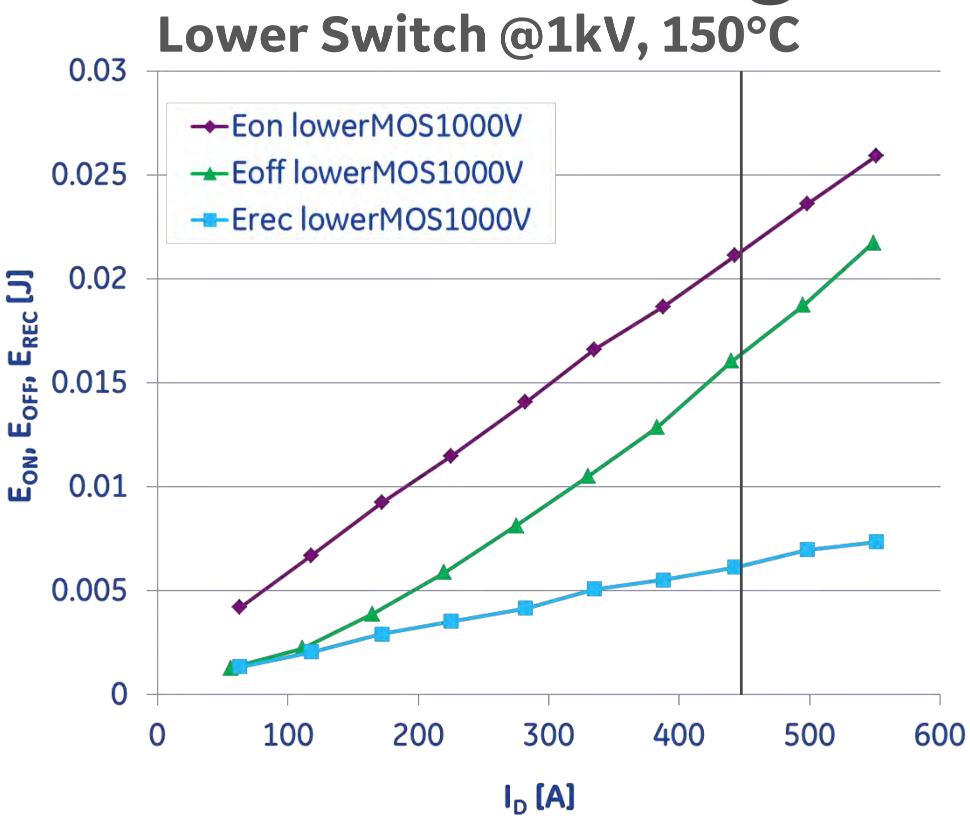
1.7kV SiC Module Switching Losses



Module Type	Switching Test Conditions	E_{ON} (mJ)	E_{OFF} (mJ)	E_{REC} (mJ)	E_{SUM} (mJ)
GE Gen-1 1.7kV SiC	1kV, 450A, 150C, $R_{ON}=R_{OFF}=4.3\Omega$	21.5	16.5	6	44
FF450R17ME4_B11	900V, 450A, 150C, $R_{ON}=R_{OFF}=3.3\Omega$	145	170	125	440

Compared to Si IGBT, SiC module switching losses are 10 times lower

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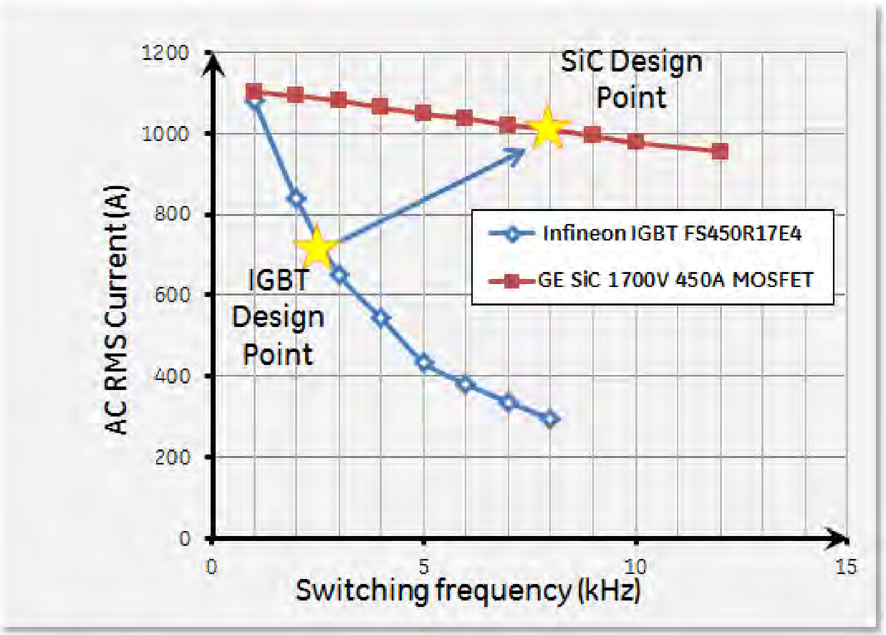
Performance and Cost Advantage

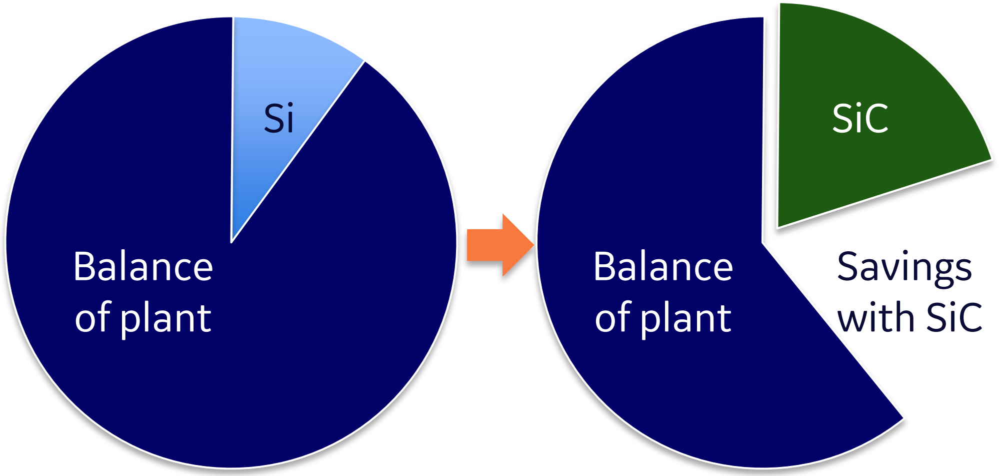
Less heat to manage	Higher temp. capability	Higher frequency
50% lower total losses vs. IGBT	25°C higher junction temp. vs. IGBT	10X higher frequency vs. IGBT



Increase current rating by 40%
at 3x higher switching frequency

Si IGBT Modules

SiC MOSFET Modules



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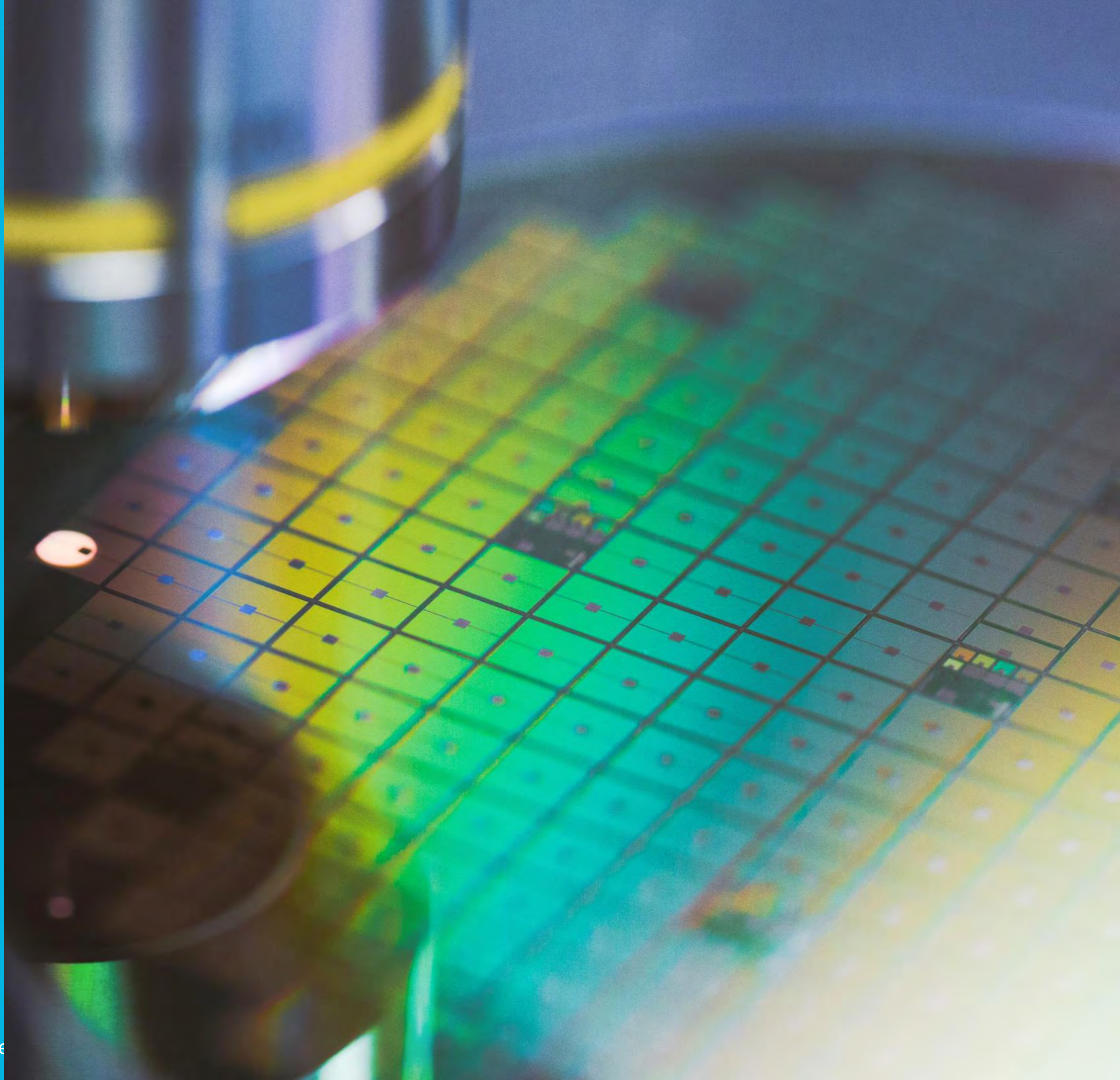
Thank you!



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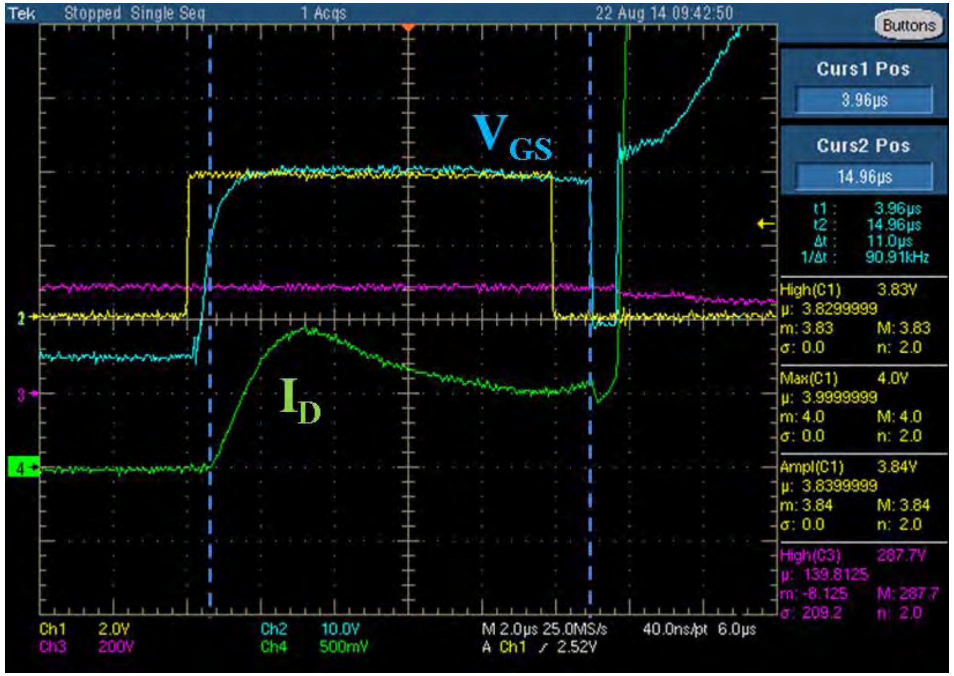
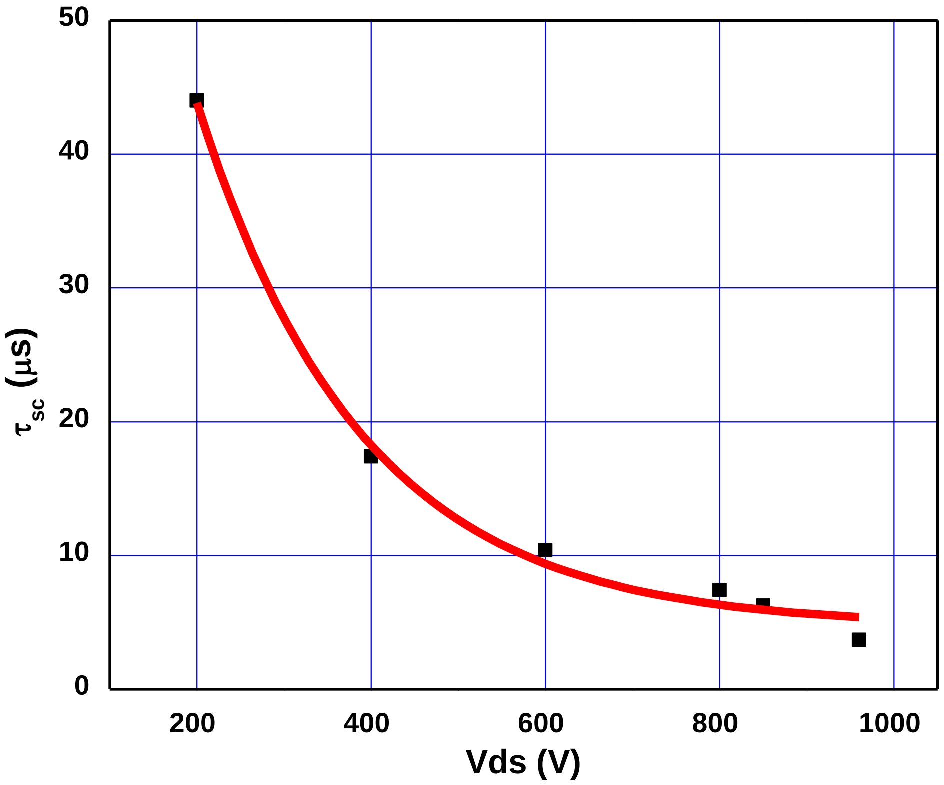
1.2kV, 30A Short-Circuit Capability

- SC capability important for system safety
- SC capability established for GE 1200V/30A MOSFET
- t_{sc} ≈10us @600V → sufficient for fault detection to react

- GE12N20L SC test example:





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1.2kV, 25mΩ MOSFET Qual Data

94A chips, TO268 package, 200°C

Test Item	Test Condition	Test Duration	4" GRC FAB RESULTS
HTGB	Temp = 200°C, VGS = 23V	1000 Hours	1 Lots: **0 / 77**
HTRB	Temp = 200°C, VDS = 960V	1000 Hours	1 Lots: **0 / 77**
MSL1	Moisture Pre-conditioning 85°C/85% RH Level 1 Prior to TC, AC, H3TRB, IOL	168 Hours	1 Lots: **0 / 308**
Thermal Shock	-55°C to 200°C Soak: >1 min Ramp: 30°C/min ±10°C	400 Cycles	1 Lots: **0 / 77**
Autoclave	96 Hrs, 121°C, 100% Rh, 15psig	400 Cycles	1 Lots: **0 / 77**
H^3TRB	85°C, 85% RH, 100V RB	1000 Hours	1 Lot: **0 / 77**
IOL	ΔT = 100°C, 2.5 min on / 5 min off	8000 Cycles	1 Lots: **0 / 77**

Results of 1200V TO268 GE1209003B1 SiC-MOSFET Qualification

AEC-Q101 Reliability Test

Test Name	Method	Condition	n (Sample Size)	Failures
Pre- and Post- Stress Electrical test	AEC-Q101	Device Specification	597	0
External Visual	JESD22 B-101	Device Specification	597	0
Parametric Verification, Picked at Random	AEC-Q101	Device Specification	25	0
Pre-conditioning	JESD22 A-113	MSL1 Prior to TC, AC, H3TRB, IOL	308	0
High Temperature Reverse Bias (HTRB)	JESD22 A-108, MIL-STD-750-1	1000 Hrs, 200°C Tj, 960V	77	0
High Temperature Gate Bias (HTGB)	JESD22 A-108 1000 Hrs	1000 Hrs, 200°C Tj, 23V	77	0
Temperature Cycling	JESD22 A-104	400 Cycles, TC -55 to 200C	77	0
TC Delamination Test	JESD22 A-104, J-STD-035	CSAM Post TC	77	0
Autoclave	JESD22 A-102	96 Hrs, 121°C, 100% Rh, 15psig	77	0
High Humidity, High Temperature Reverse Bias (H3TRB)	JESD22 A-101	1000 Hrs, 85°C/85% RH, 100V	77	0
Intermittent Operational Life (IOL)	MIL-STD-750 Method 1037	100°C Δ Tj	77	0
ESD Characterization (CDM,HBM,MM)	AEC-Q101	001, 002, 005	90	H2, M4, C5
Destructive Physical Analysis	AEC-Q101-004	POST TC, H3TRB, IOL	9	0
Physical Dimension	JESD22 B-100	Device Specification	10	0
Solderability	J-STD-002	Eutectic SnPb, 235°C	10	0
Thermal Resistance	JESD24-3	Device Specification	10	0
Wire Bond Strength	MIL-STD-750 Method 2037	Min. 28g Gate, Min. 130g Source	5	0
Bond Shear	AEC-Q101 -003	Min. Tensile Strength of Wire	5	0
Die Shear	MIL-STD-750 Method 2017	Min. 5kG	5	0
Unclamped Inductive Switching	AEC-Q101-004 Section 2	Device Specification	5	0
Dielectric Integrity	AEC-Q101-004 Section 3	Device Specification	5	0

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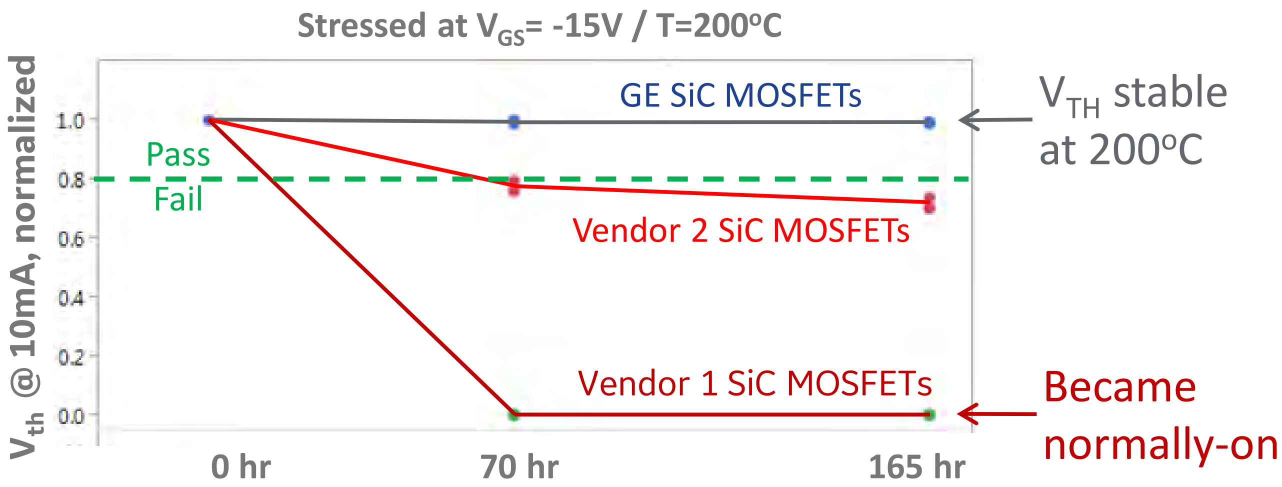
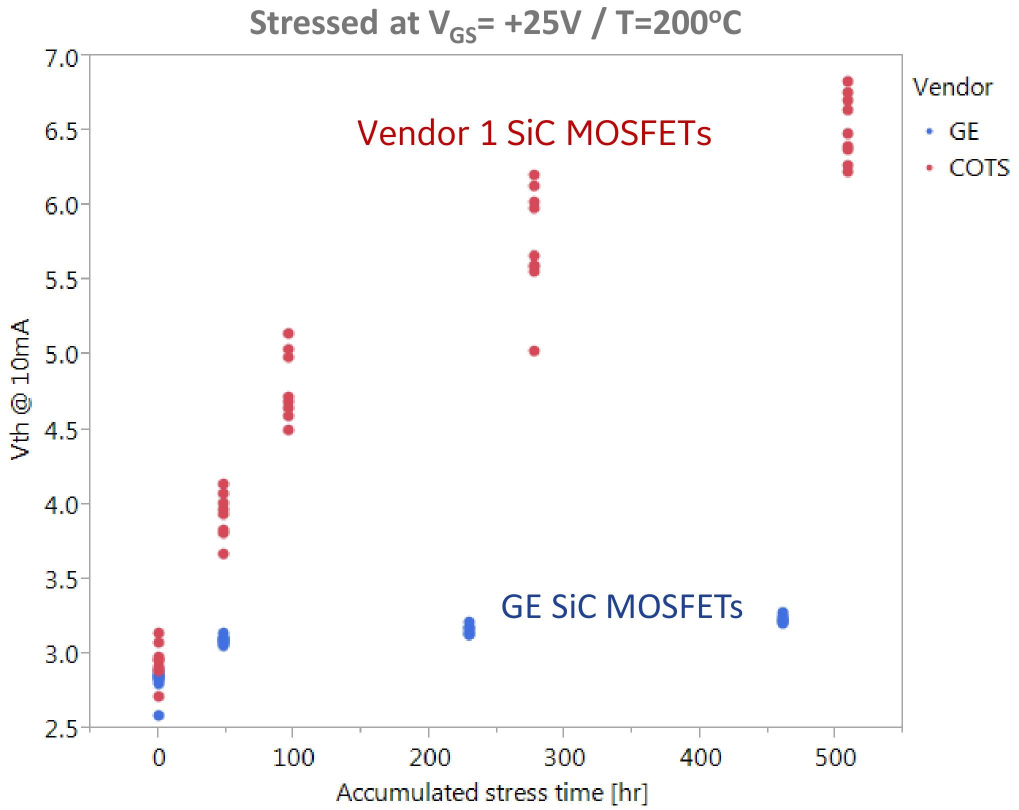
Competitive Benchmarking: SiC MOSFET V_{th} Stability

Negative Bias Threshold Instability (NBTI)



Positive Bias Threshold Instability (PBTI)



GE MOSFET V_{th} stability enables 200ºC rating

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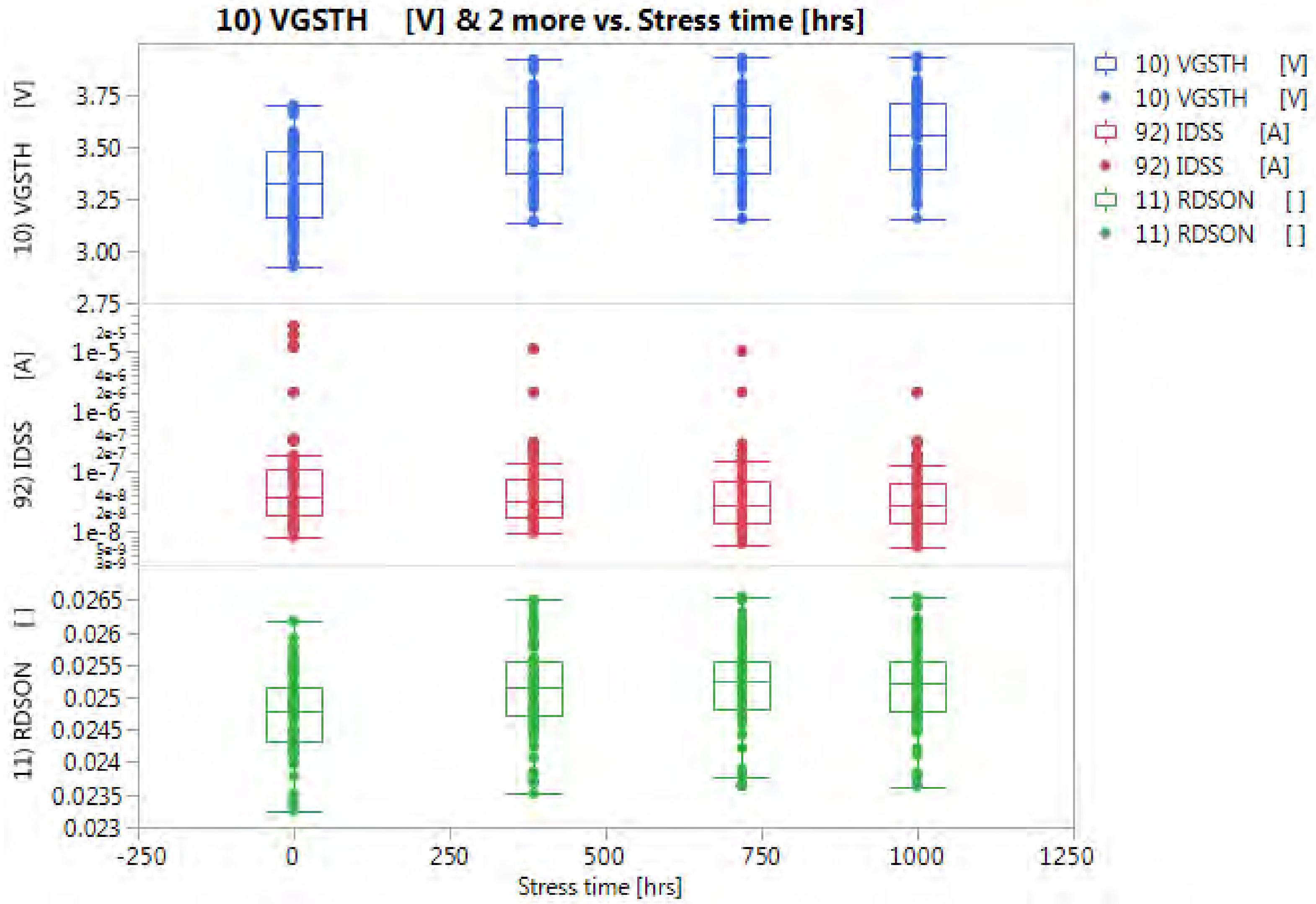
GE 1.2kV, 25mΩ MOSFET Qual Test: 1000-hr HTGB @ +23V, 200°C



GE MOSFET key parameters stable at 200°C

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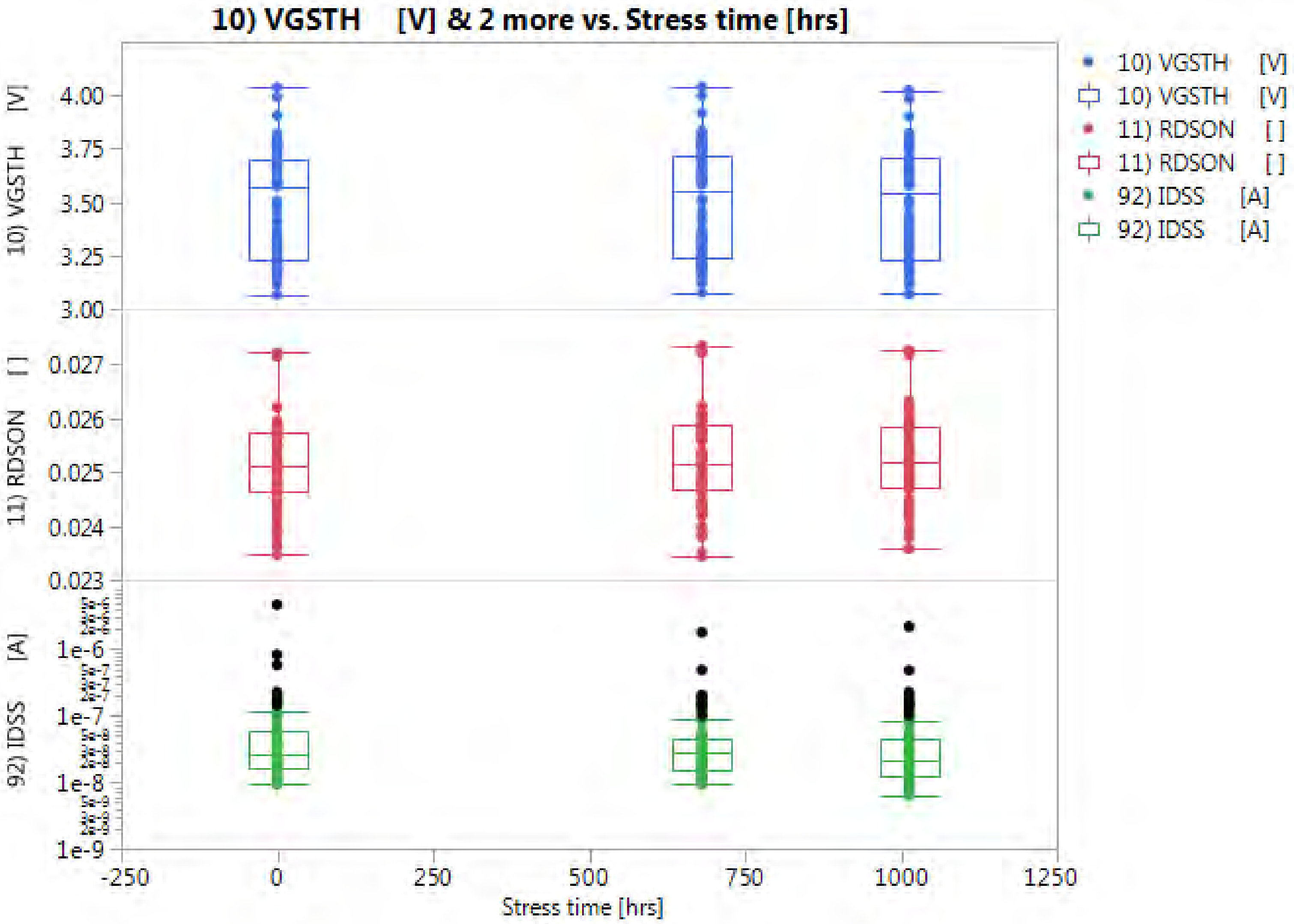
GE 1.2kV, 25mΩ MOSFET Qual Test: 1000-hr HTRB @ 960V, 200°C



GE MOSFET key parameters stable at 200°C

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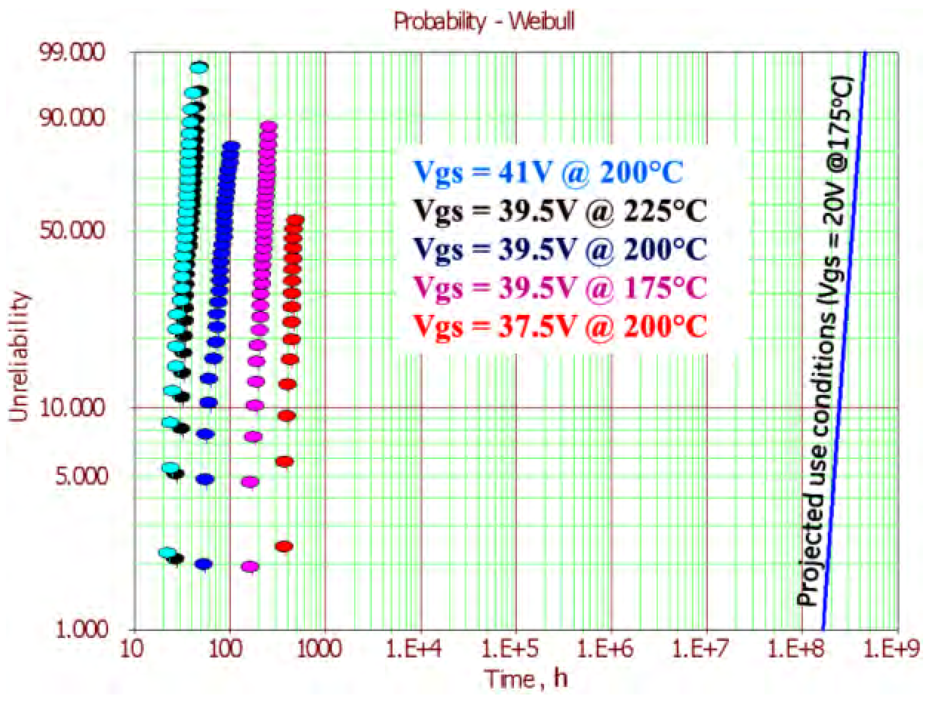
Gate Oxide Lifetime Model

Developed using full MOSFETs

Highly accelerated life testing:

- 41V, 39.5V, 37.5V @ 200°C
- 39.5V @ 175°C
- 39.5V @ 225°C



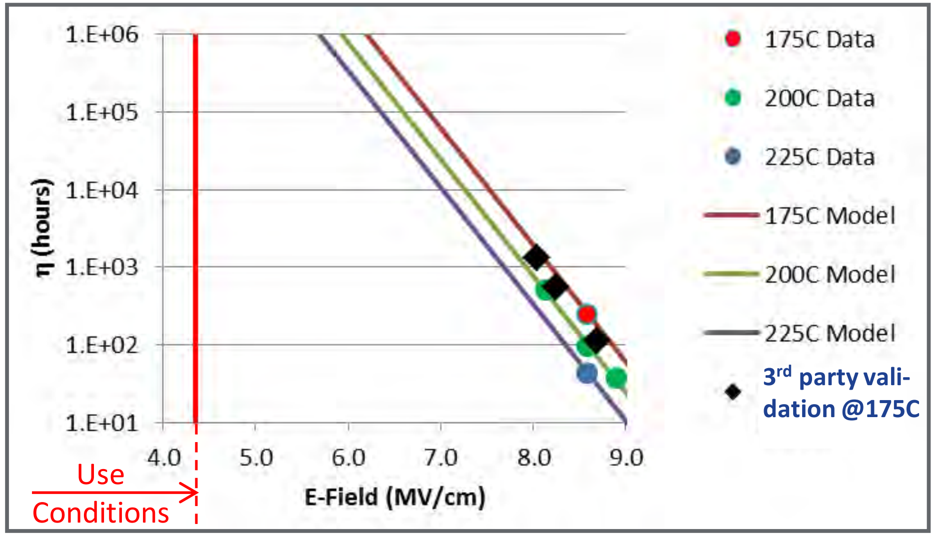
is used to derive lifetime model:

$$T_{LIFE,63\%} = e^{\alpha_0+\alpha_1\times E_{FIELD}+\alpha_2/kT}$$

which can be applied to predict gate oxide life at projected use-conditions:

- 20V @ 175°C
- η = 0.6*10^9 hrs

Conclusion: oxide life exceeds100 yr target



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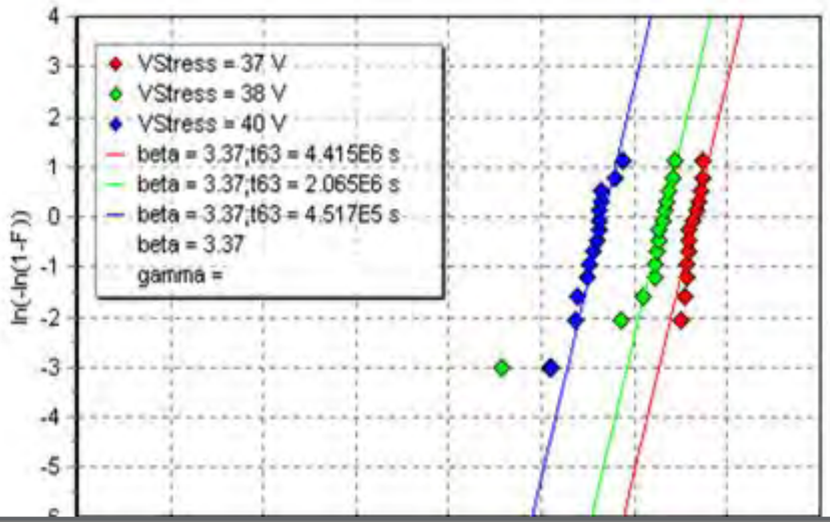
3rd Party TDDB Testing of GE MOSFETs

41 samples of TO247-packaged 1.2kV, 30A Gen-1 (GE12N20L) parts

Results:

- gamma = xx cm/MV
  (assuming t_ox = x nm)
- Steep distributions (beta = 3.4)
- SiC-MOSFETs show comparable behaviour to Si-MOSFETs



"Great results, congratulations!"

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